

Analog Signal Processing

ATLAS CSC Electronics

Conceptual Design Review

Aug. 7, 2000

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Outline

- **Signals and noise - theory**
- **Implementation:**
 - **organization**
 - **mechanics**
 - **circuitry**

Signal formation, noise, and gain - 1

1. Chamber electrode configuration

- 4 gas gaps
- 192 precision strips
 - Readout pitch $d = 5.547\text{mm}$
 - Cstrip 20 – 50 pF
- 48 transverse strips (no interpolation)
- anode wires
- Outer "skin" of chamber is GROUND with firm connection to Faraday shields
- Each gap has perimeter ground
- Perimeter grounds linked across top of chamber, to skins

2. Signal size

- muon generates 75 electron-ion pairs (Landau peak)
- gas gain $\sim 10^5$
- 12% of charge is collected by the precision cathode in 100 ns
- => signal size is $\sim 900,000 e^-$ (144 fC) $\equiv Q_\lambda$
- central strip of cluster receives $\sim 1/2$ of charge => 72 fC ($Q_{\lambda,\text{cent}}$)

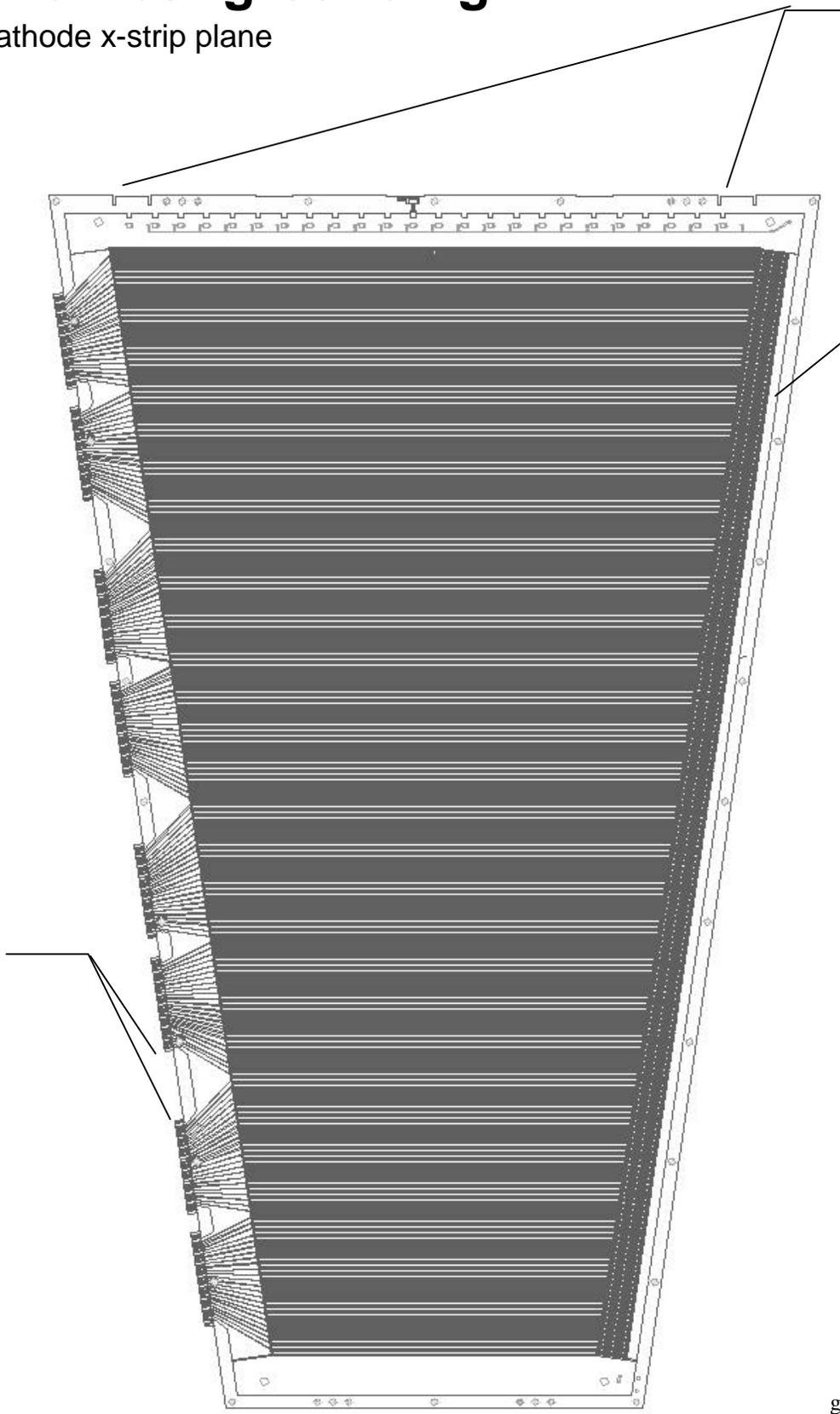
Chamber grounding

Cathode x-strip plane

Ground connection to other 3 x-strip planes

Continuous ground ring around outside edge of cathode planes

Ground connection to ASM-I's



Signal formation, noise, and gain - 2

3. Noise

- electronics noise shouldn't degrade position resolution

$$s_{x,elec} = \frac{\sqrt{3} \cdot d \cdot ENC}{Q_1} \leq 33mm$$

where d = strip pitch, ENC = equivalent input noise charge, Q = charge induced on cathode plane

$$ENC \leq 0.5 fC = 3100e^- \leftarrow \text{TOTAL input referred noise}$$

$$\text{Signal-to-noise (max. strip)} = \frac{Q_{1,cent}}{ENC} = \frac{72 fC}{3100e^-} = 145$$

4. Dynamic range and gain

for 98.5% efficiency,

$$\frac{Q_{FS}}{Q_1} \geq 5$$

$$\therefore Q_{FS} \geq 5 \cdot Q_1 = 725 \cdot ENC \cong 360 fC$$

for preamp/shaper $V_{FS} = 1.7$ V (positive lobe of bipolar waveform)

$$\therefore P/S \text{ gain} = \frac{V_{FS}}{Q_{FS}} = 4.7 mV / fC$$

5. Quantization

$$\frac{Q_{FS}}{2^{Nbits} \cdot \sqrt{12}} \ll ENC$$

$$2^{Nbits} \gg \frac{Q_{FS}}{\sqrt{12} \cdot ENC} = 209$$

$$Nbits \gg 7.7$$

$$Nbits = 10 (s_{Q,quant} = 20\% ENC) \text{ or } 12 (s_{Q,quant} = 5\% ENC)$$

12 bits preferred to accommodate negative lobe, gain and offset variations, etc.

High Rate / High Background Operation

- Overall background rate 10^7 Hz per chamber
- 50% charged particles, 50% neutron and γ
- Charged particle background is rejected by timing window around trigger or by pattern recognition of non-projective tracks
- Neutrals can deposit high charges:
 - 50% of neutrals above Q_{FS}
 - 1% of neutrals above $6 \times Q_{FS}$
- Neutrals produce short-range electrons so usually confined to 1 layer only
- But a neutral hit anywhere in chamber induces charge on all strips by anode-cathode crosstalk:

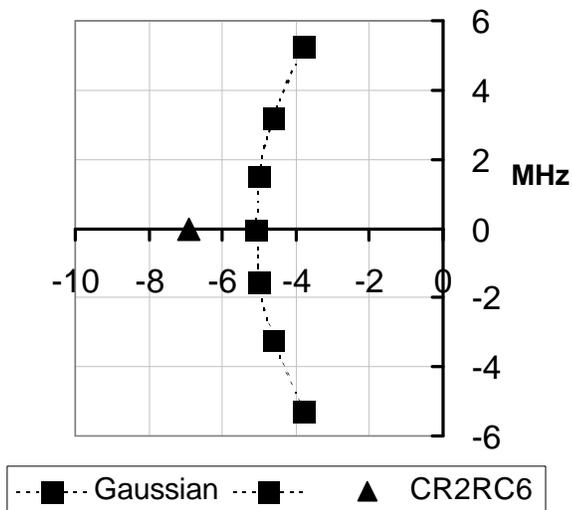
$$Q_{cross} = \frac{C_{ac}}{C_{filt}} \cdot Q_{anode} \cong 10^{-4} Q_{anode}$$

- This high-rate, low amplitude background behaves like electronic parallel noise (choice of shaping function)
- Within-chip crosstalk distorts signals in cluster, can systematically shift interpolated centroid position.

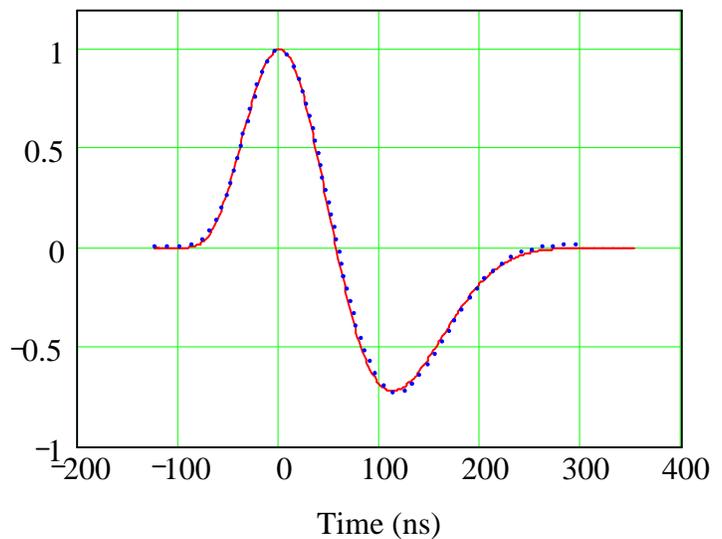
Rates and pulse shaping

- Optimal pulse shaping is a compromise between noise, which degrades position resolution, and pileup, which contributes to inefficiency.
- Bipolar pulse preferred in high-rate environment.
- From Monte Carlo study, peaking time should be ~ 100 ns and $FW1\%M < 430$ ns
- Bipolar 7th-order shaper using complex poles gives same return to baseline as 12th-order CR^2-RC^n configuration

Shaper Pole Positions

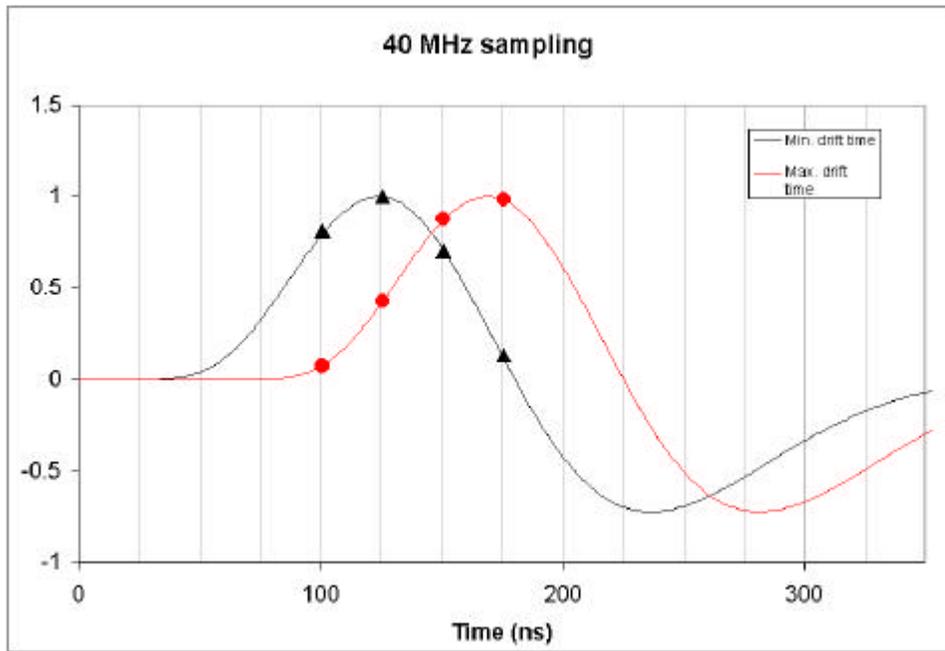


Waveform

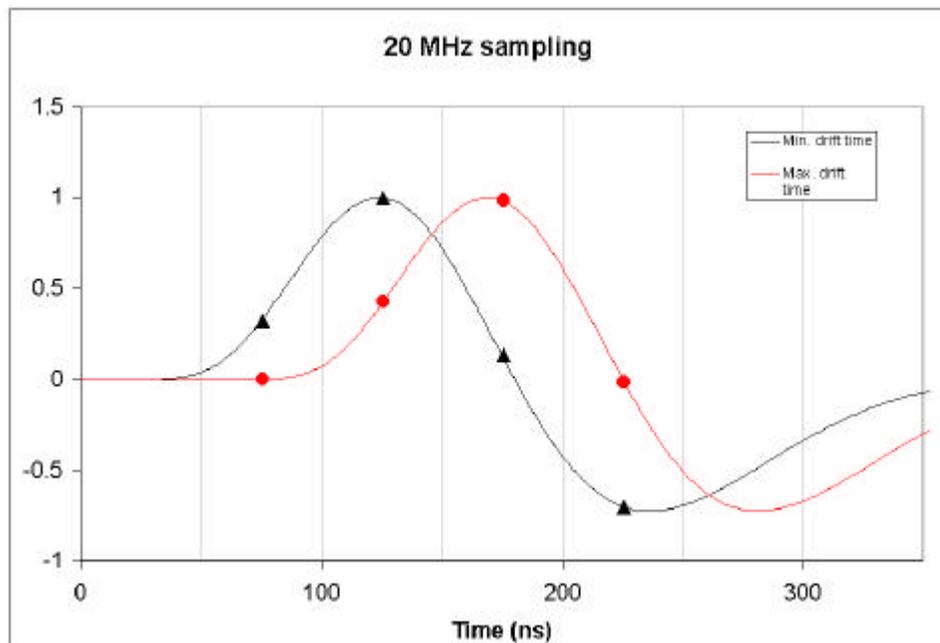


Sampling rate

- With 40 MHz sampling and only 4 samples, we can't always get the peak and both neighbors



- 20 MHz sampling/4 samples gives a wider window and doesn't degrade the resolution or efficiency



Calibration

- Precise (0.5%) calibration is necessary for interpolation
- Each plane has calibration circuit on ASM-II
- Pulse wire groups to induce charge on all strips simultaneously

$$0 \leq Q_{\text{cal}} \leq Q_{\text{FS}}$$

- Circuit still under development

Reliability

Goal: < 0.1% data lost due to hard or soft fails

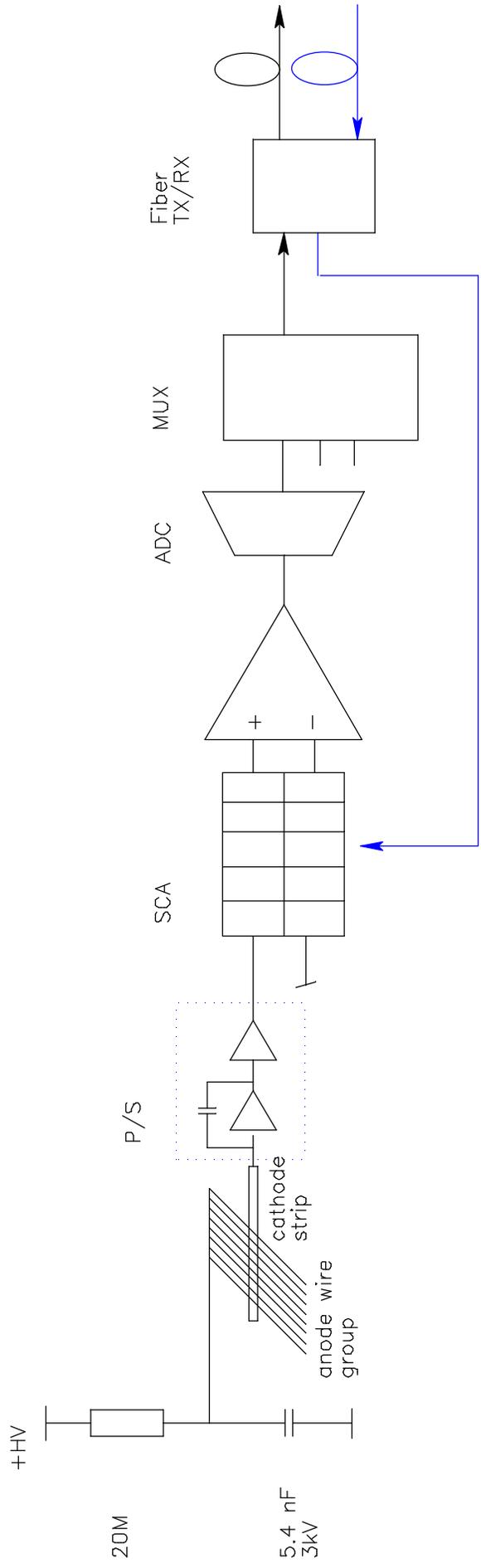
Strategy: on-detector electronics boards must be as simple and robust as possible

- Minimal parts list: B.O.M. for ASM-PACK active components:

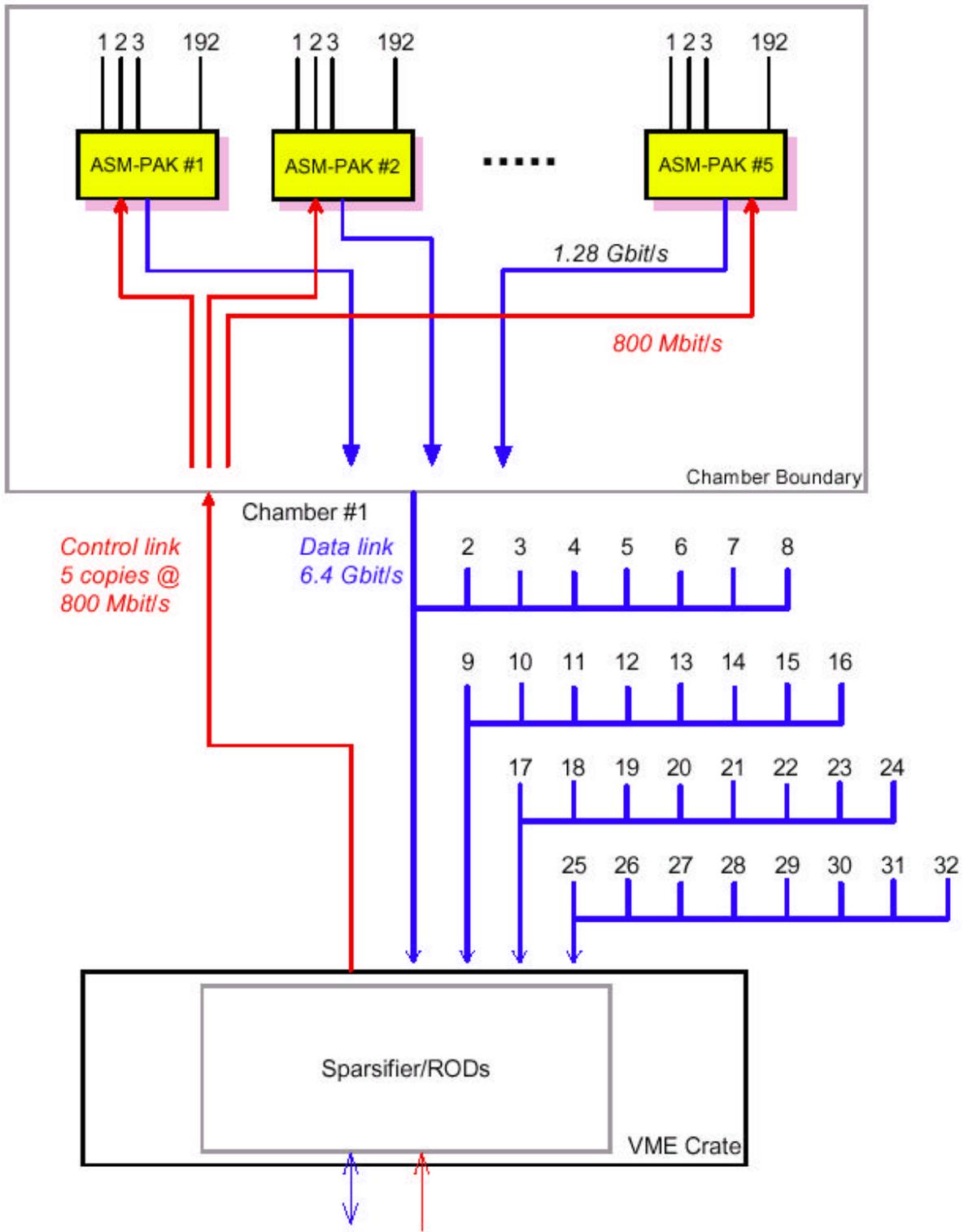
<i>3.3V (adj) regulator</i>	<i>AD 9042 12-bit ADC</i>
<i>5V fixed regulator</i>	<i>10H116 PECL driver</i>
<i>IC50 custom preamp/shaper</i>	<i>1N914 protection diodes</i>
<i>HAMAC v.4 custom SCA</i>	<i>G-link transceiver</i>
<i>AD8042 dual op-amp</i>	<i>HDMP 1022/1024 serializer/deserializer</i>
- All intelligence to reside on sparsifier/ROD
- ASM to have no

<i>Configuration registers</i>	<i>Programmable logic</i>
<i>FIFOs</i>	<i>RAM</i>
<i>Counters</i>	<i>State machines</i>
- Thorough radiation test of all components
- ESD protect inputs at board and chip level
- ATLAS policy on grounding and shielding
- Extra attention to amplifier stability
- No DCS
- Minimal monitoring

CSC Electronics Analog Signal Chain



CSC Electronics Overall Organization



CSC Electronics Numerology

SYSTEM

- 2 endcaps
- 64 chambers
- 61,440 channels
- 640 ASM-PACKs
- 32 Sparsifier/RODs

CHAMBER

- 4 layers
- 960 channels (768 precision, 192 transverse)
- 5 ASM-PACKs
- 15 optical links (10 data, 5 control)

ASM-PACK

- 192 channels
- 1 ASM-II board
- 2 ASM-I boards
- 3 fiber optic links

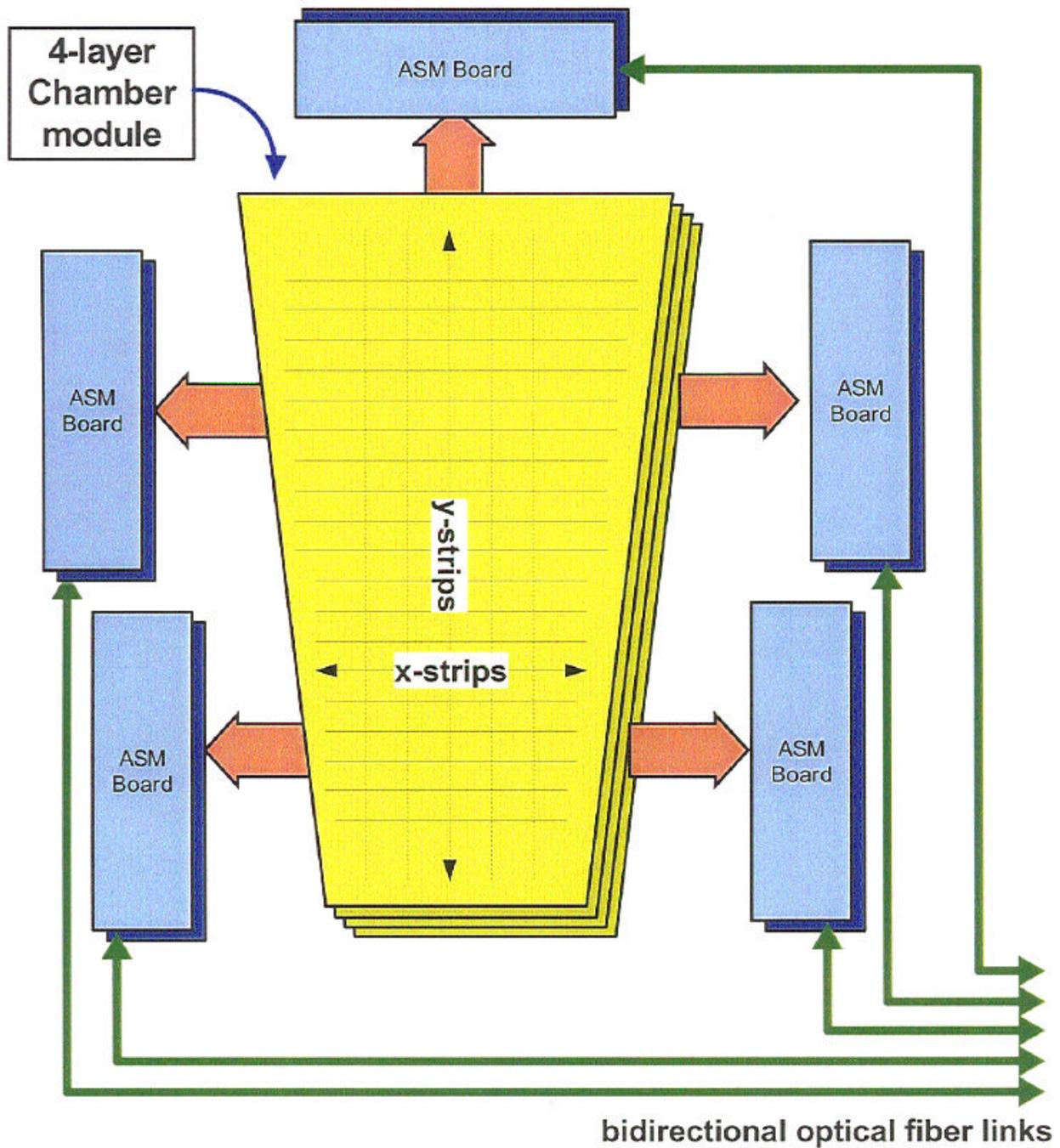
ASM-II

- 192 channels
- 2 ASM-I's
- 16 SCA ASICs
- 16 ADCs
- 2 serializer/transmitters
- 1 receiver/deserializer

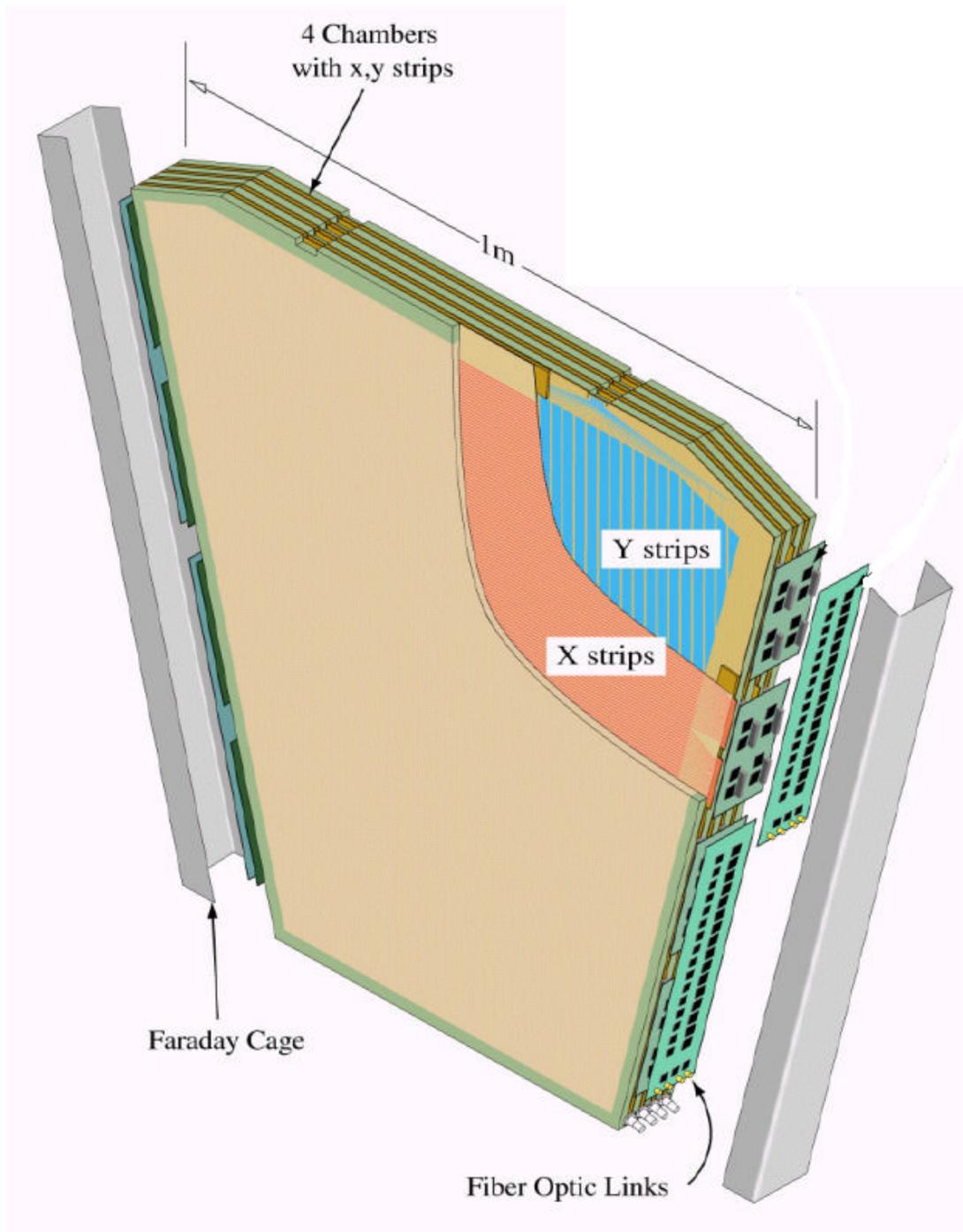
ASM-I

- 96 channels
- 16 Preamp/Shaper ASICs

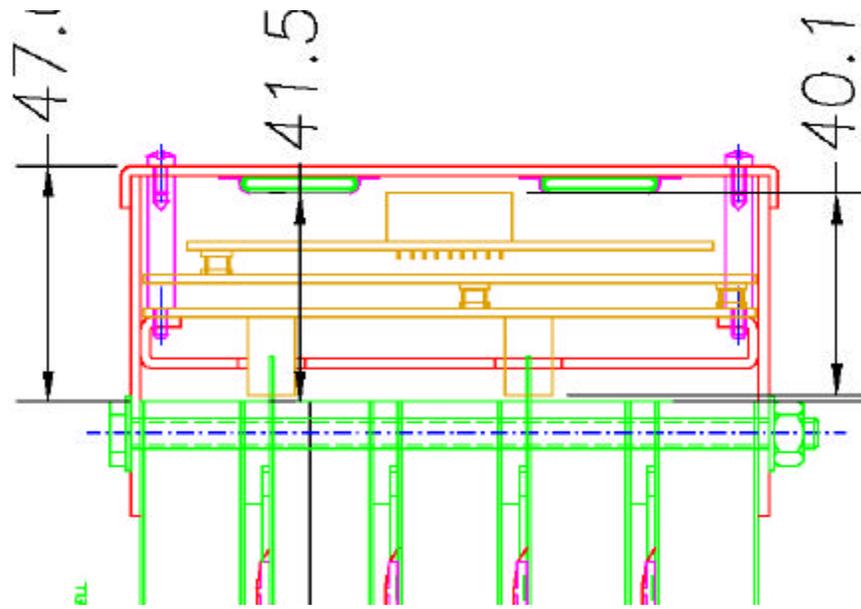
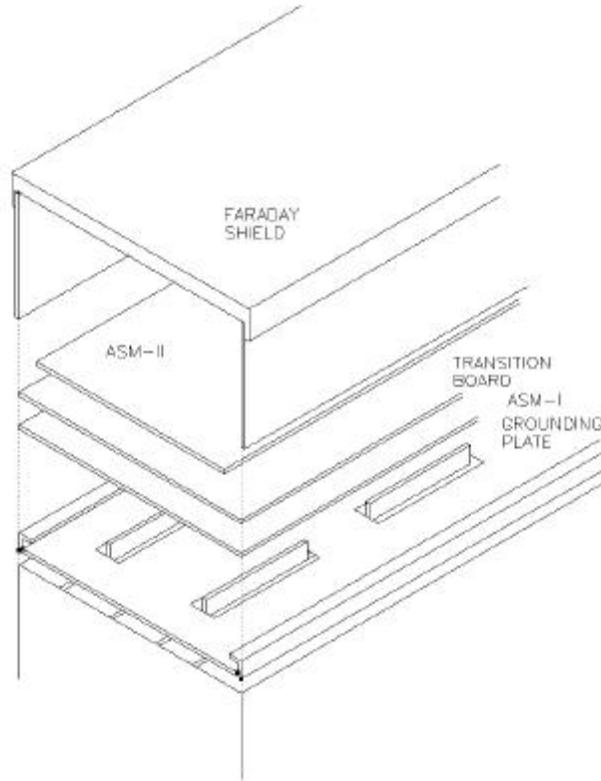
CSC On-Detector Electronics



CSC Mechanics

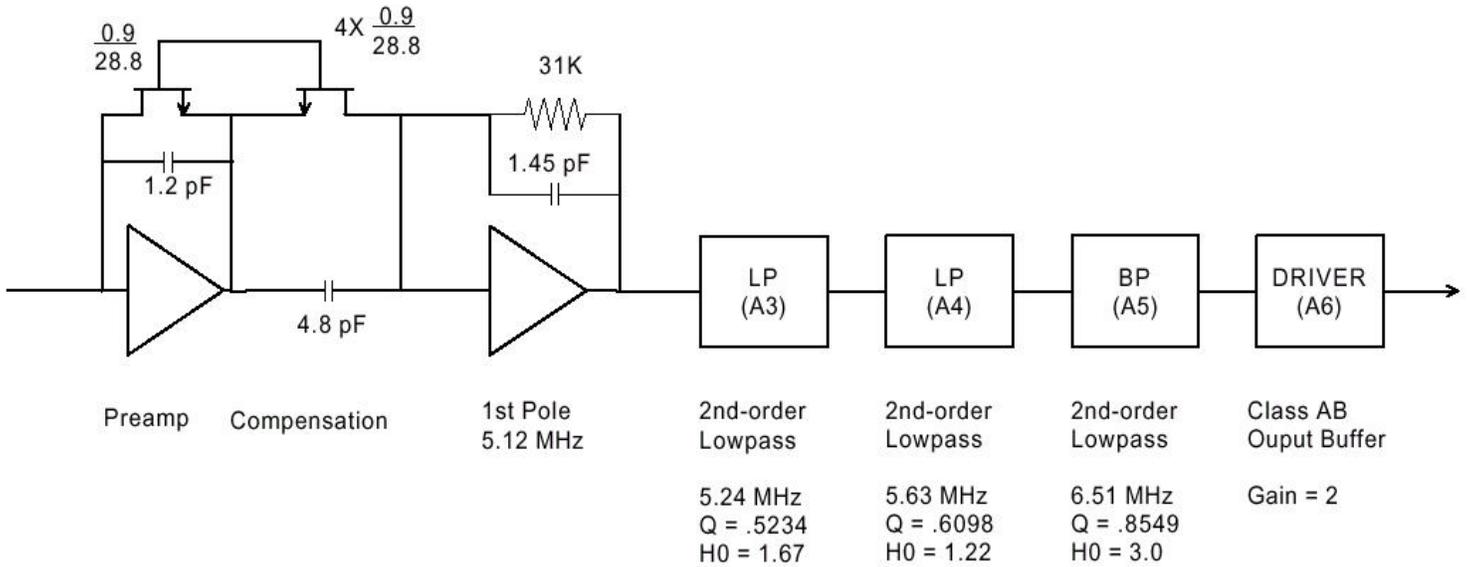


CSC On-detector Electronics Mounting



CSC Preamplifier/Shaper IC (IC50)

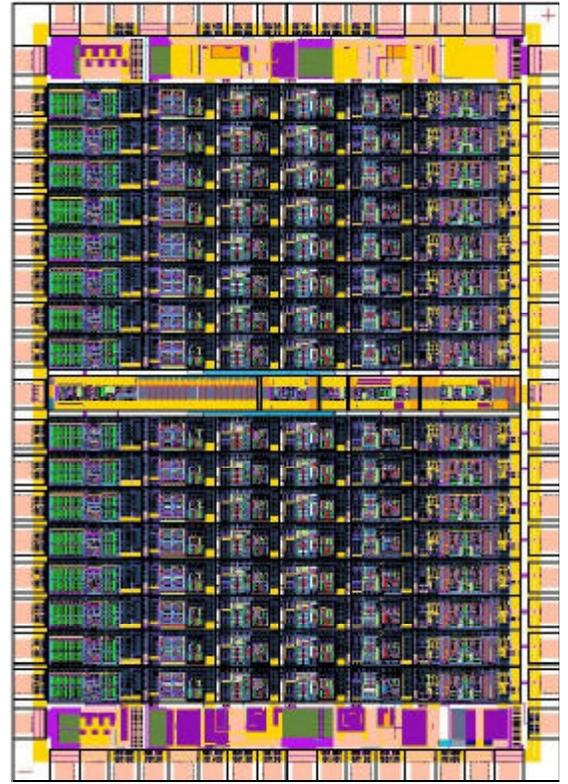
Block Diagram



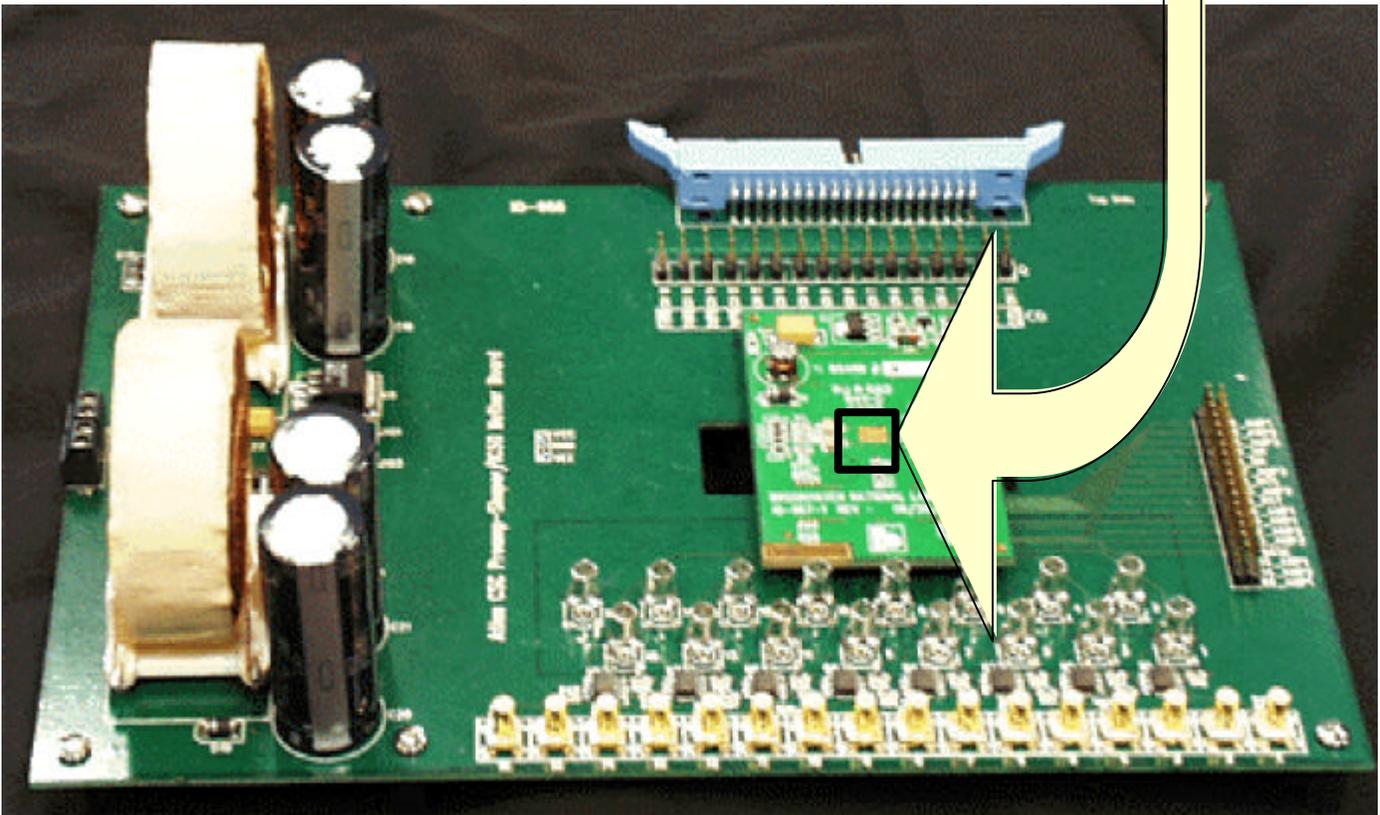
Technology	0.5 μ m CMOS
Channels	16
Die size	2.78 x 3.96 mm
Architecture	Single-ended
Intended Cdet	20 – 100 pF
Input device	NMOS W/L = 5000/0.6 μ m, Id = 4mA
Noise	1140 + 17.6 e-/pF
Gain	3.8 mV/fC
Max. linear charge	450 fC
Class AB Output swing	To power supply - 250 mV
Pulse shape	7 th order complex Gaussian, bipolar
Pulse peaking time, 5% - 100%	73 ns
FW1%M	340 ns
Max. output loading (3% distortion)	500 Ω , 500 pF
Crosstalk	0.8% adjacent, 0.5% non-adjacent channel
Power supply	Single +3.3V
Power Dissipation	32.5 mW/chan

CSC Preamp/shaper

Die Layout

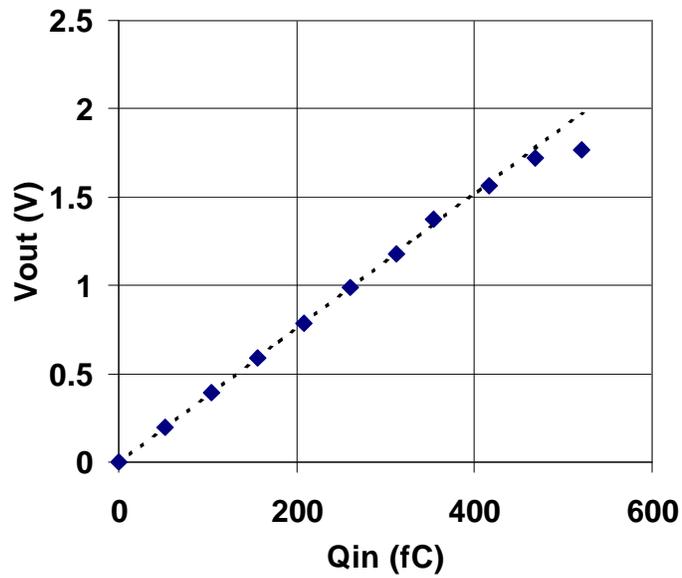


Test board

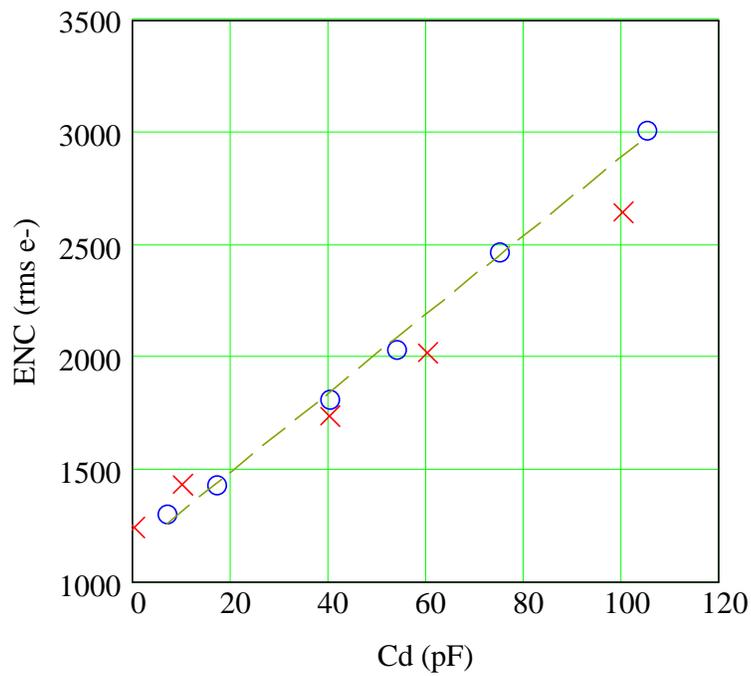


Preamp/Shaper Results

Linearity



Noise vs. capacitance



Simulated: x

Measured: o

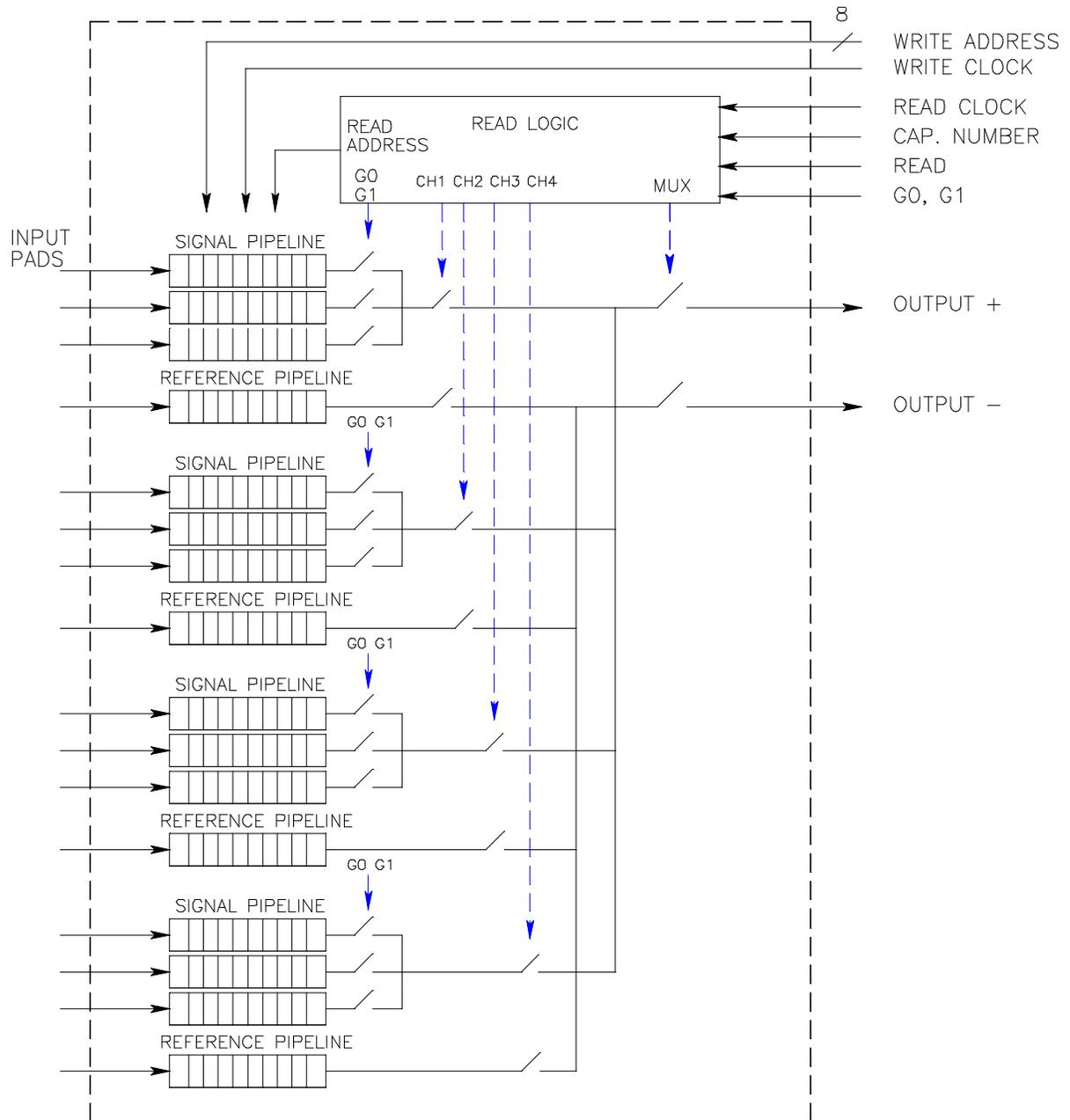
SCA Block Diagram

144 cells/channel

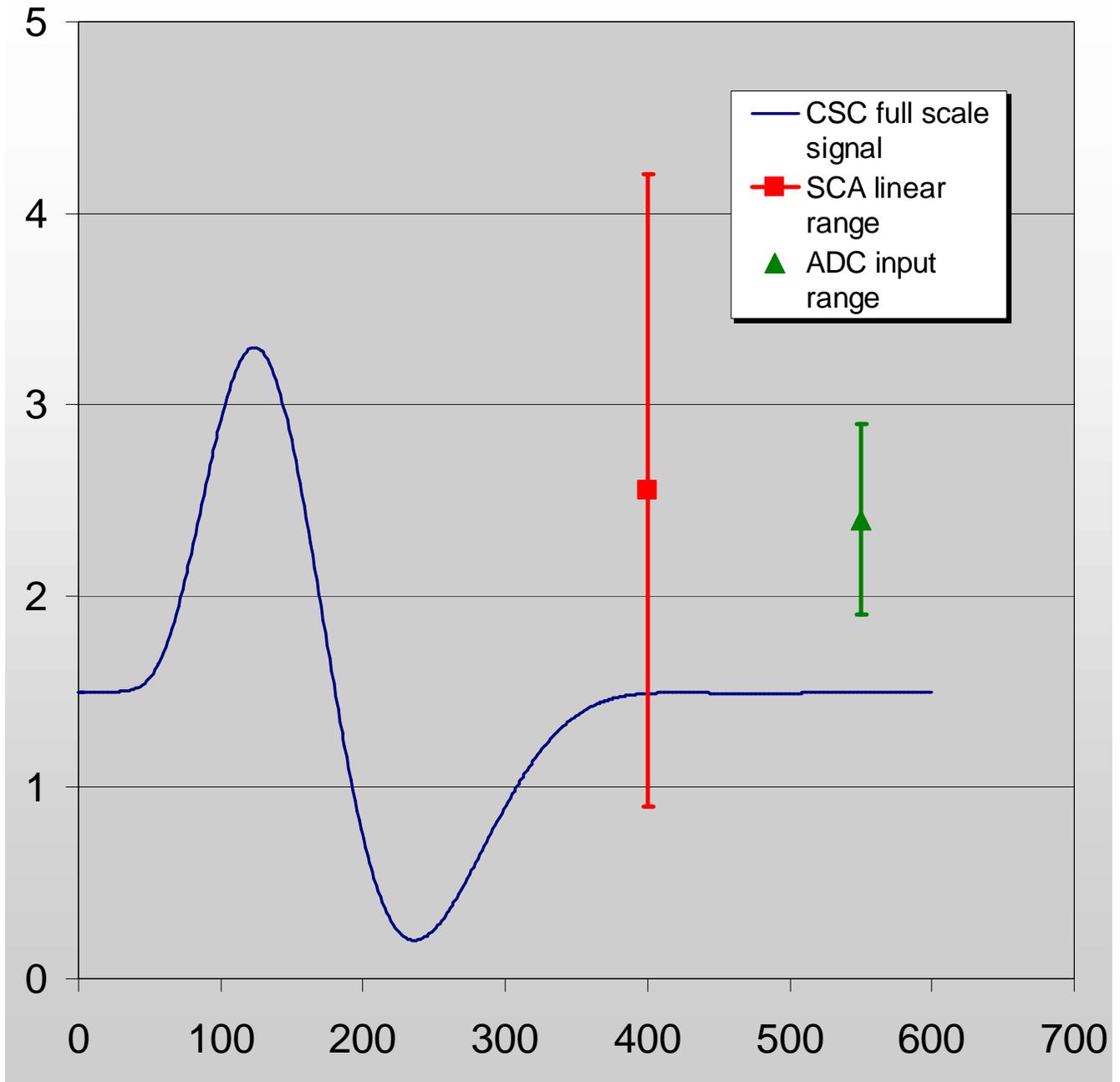
16 channels, organized as 4 groups of (3 + 1 reference)

Simultaneous read and write (deadtimeless)

Read logic modified 5/99 for CSC

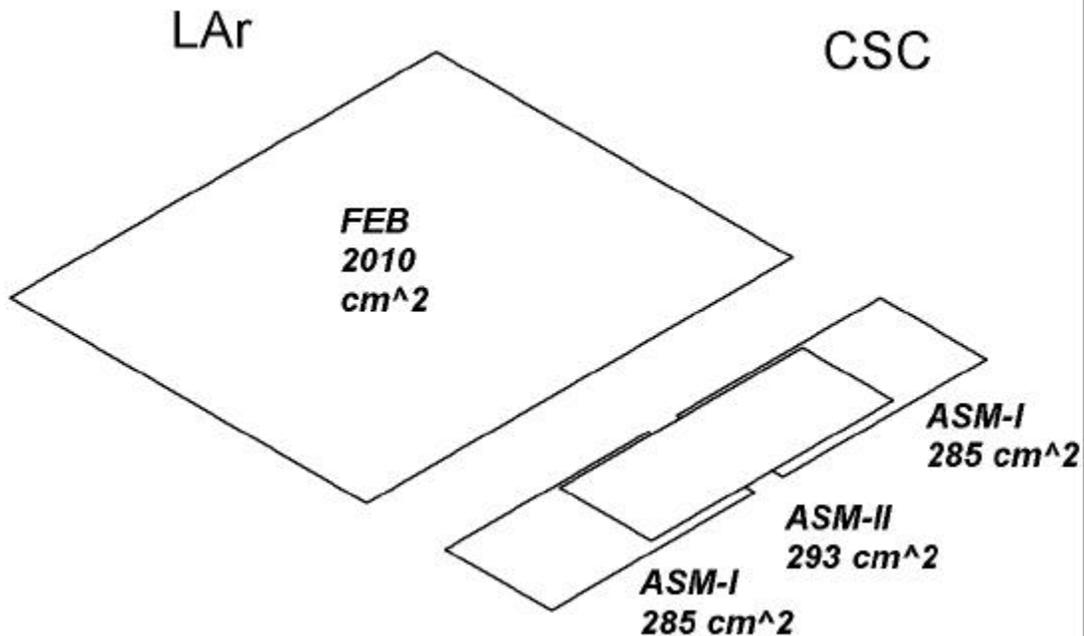


Signal levels in the CSC



Comparison of the LAr FEB and the CSC ASM-PACK

	LAr-FEB	CSC-ASM	Units
Channels	128	192	-
Gain ranges	3	1	-
Total board area	2010	580	cm ²
Signal levels:			
<i>baseline</i>	0.0	+1.5	V
<i>max.</i>	+2.5	+3.2	V
<i>min.</i>	-0.9	0.0	V
Power dissipation	85	35	W
Sampling rate	40	20	MHz
No. samples/trigger	5	4	-
Bits/sample	12	12	-
Raw data rate	896	922	Mbits/s



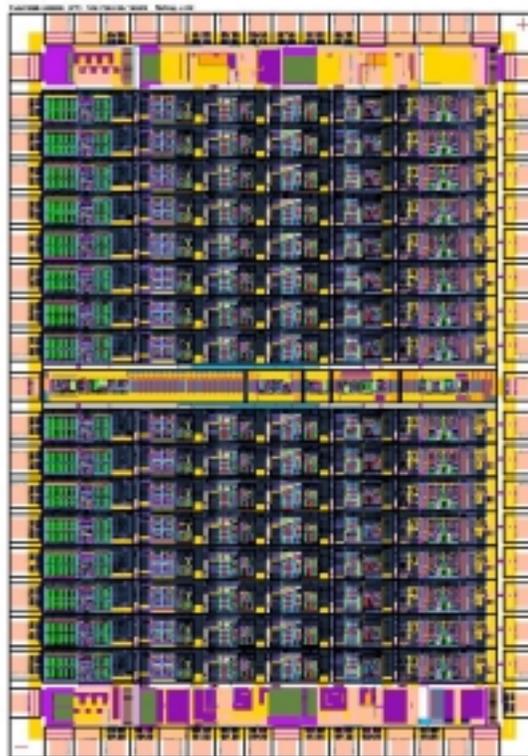
Summary – CSC On-detector Electronics

- Analog signal processing tuned for good S/N in ATLAS high rate, high background environment
- 10-b dynamic range
- Analog memory for data buffering with minimal deadtime
- SCA, digitization, data link based on LAr calorimeter system but with remote controller
- Engineered for robustness and reliability by minimizing hardware in this inaccessible, high radiation location

ATLAS Cathode Strip Chamber Preamplifier Shaper Integrated Circuit (IC50) Prototype Test Results (April 2001)

Specifications:

Channel count : 16
Process: Agilent Technologies 0.5 μ m AMOS14TB Process
Gain: 4 mV/fC
Shaping: 70ns/Bipolar
Die size: 2.78mm x 3.95mm

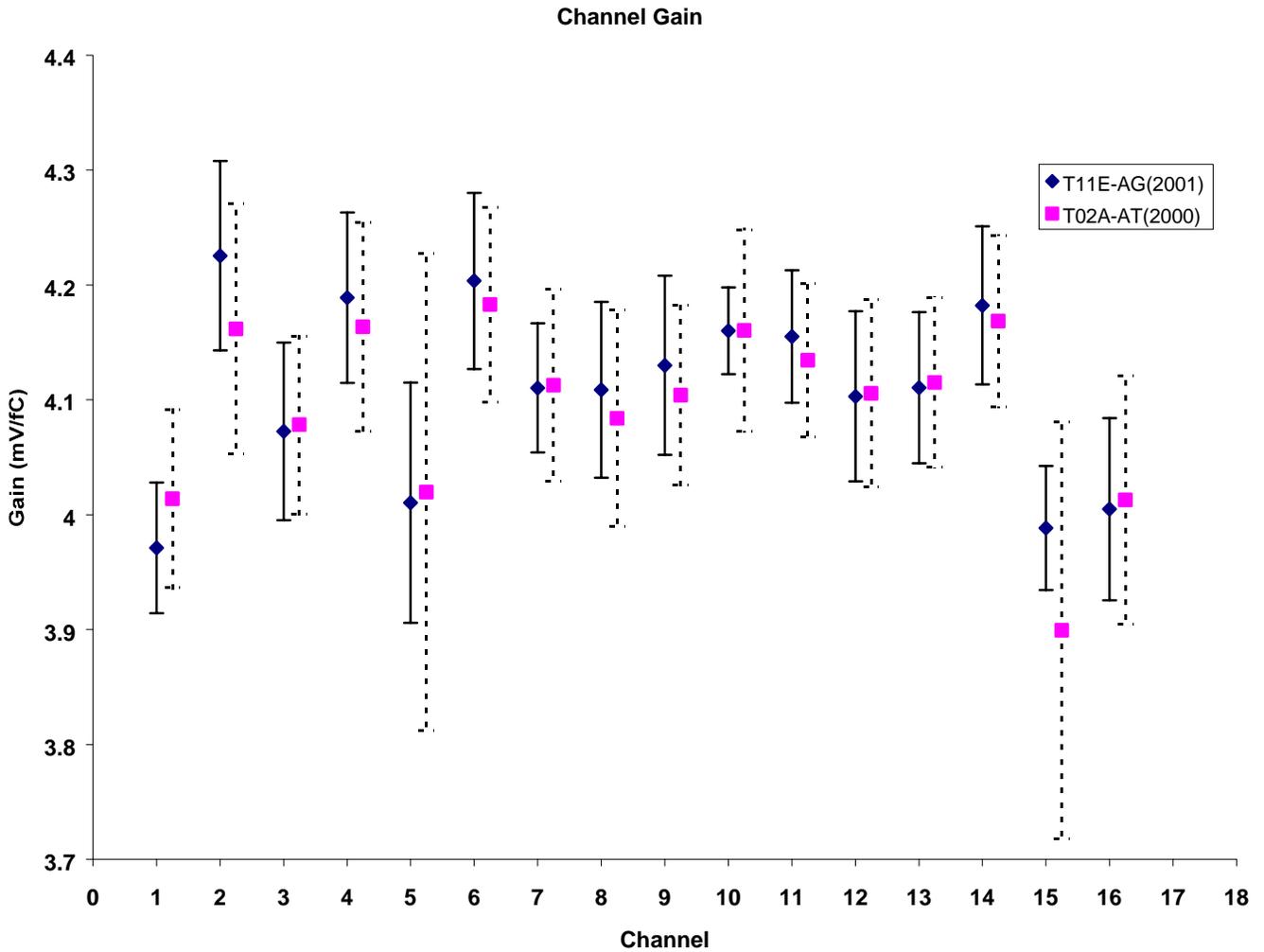


Prototyping Runs:

RUN ID	YEAR	QTY
N95C-AR	2Q – 1999	25
T02A-AT	1Q – 2000	32
T11E-AG	1Q – 2001	25

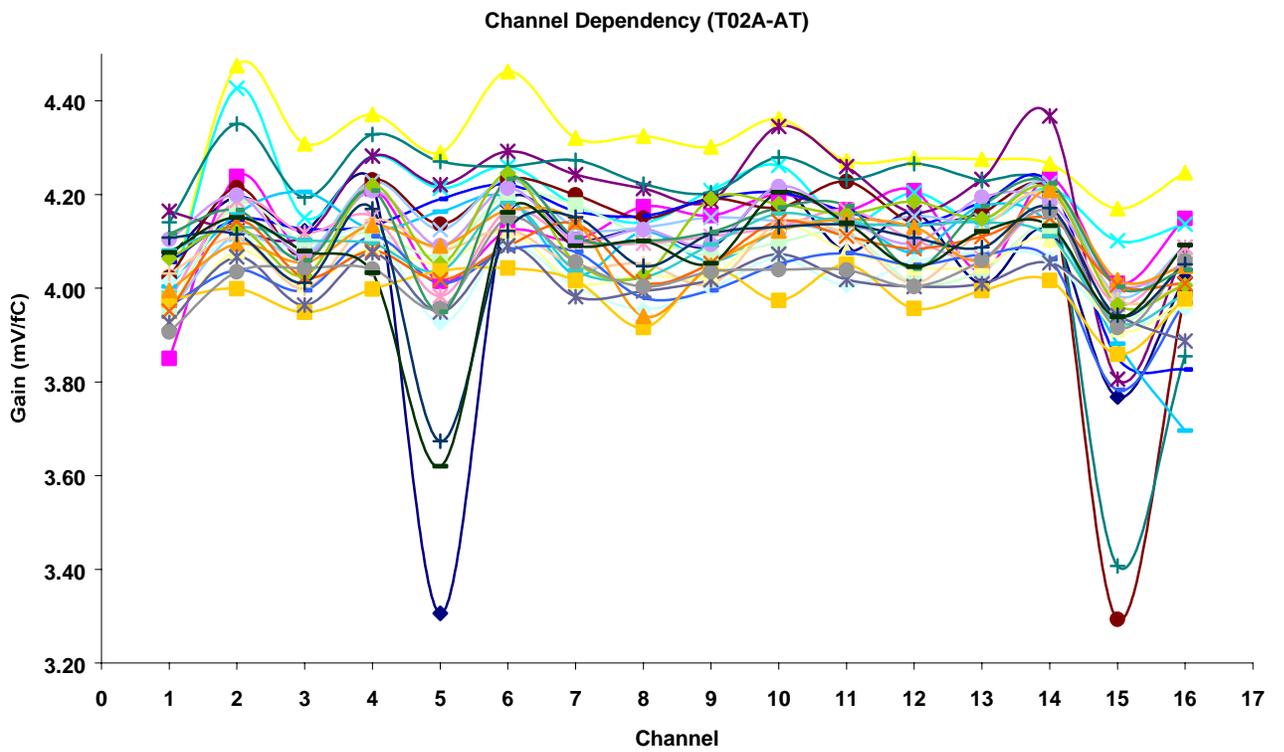
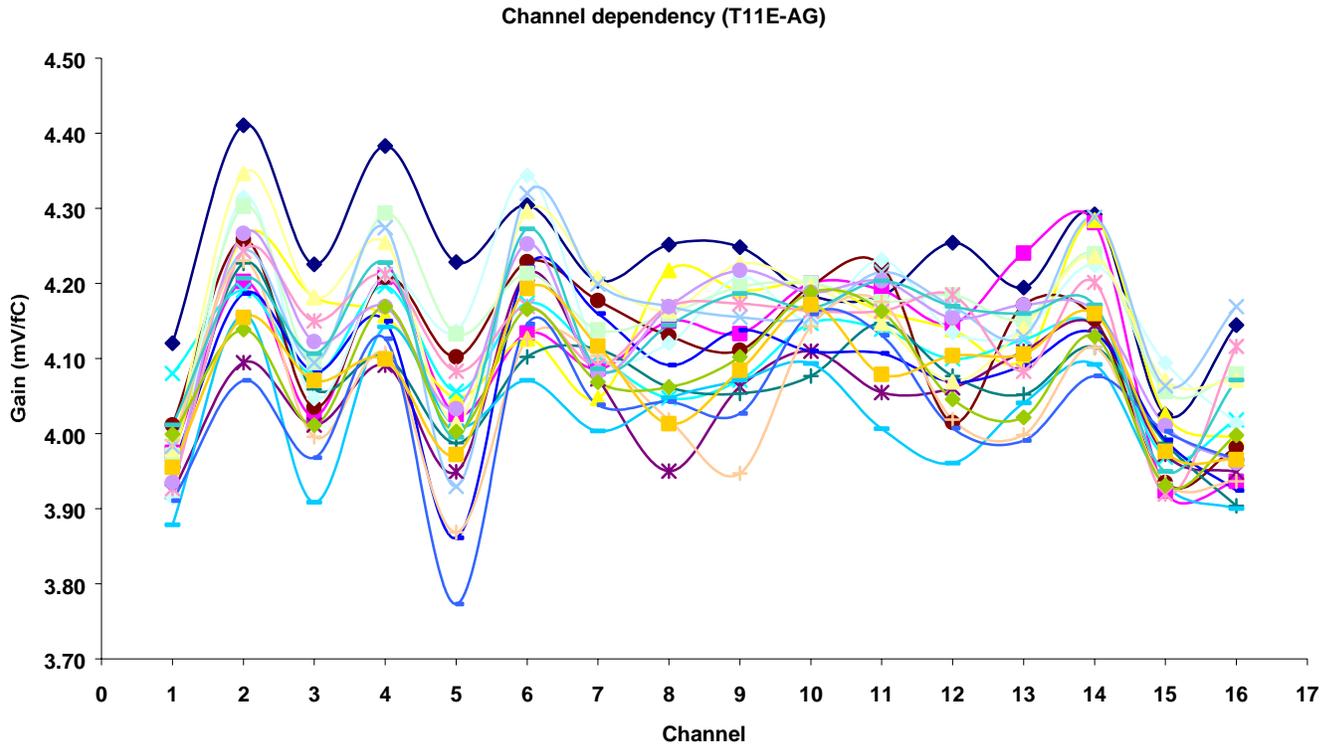
Gain:

	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15	Ch16
T11E	3.97	4.23	4.07	4.19	4.01	4.20	4.11	4.11	4.13	4.16	4.16	4.10	4.11	4.18	3.99	4.00
	1.43%	1.95%	1.90%	1.77%	2.61%	1.82%	1.37%	1.86%	1.89%	0.91%	1.39%	1.81%	1.60%	1.64%	1.35%	1.98%
T02A	4.01	4.16	4.08	4.16	4.02	4.18	4.11	4.08	4.10	4.16	4.13	4.11	4.12	4.17	3.90	4.01
	1.93%	2.62%	1.90%	2.18%	5.16%	2.03%	2.03%	2.31%	1.91%	2.11%	1.61%	1.99%	1.80%	1.79%	4.66%	2.70%



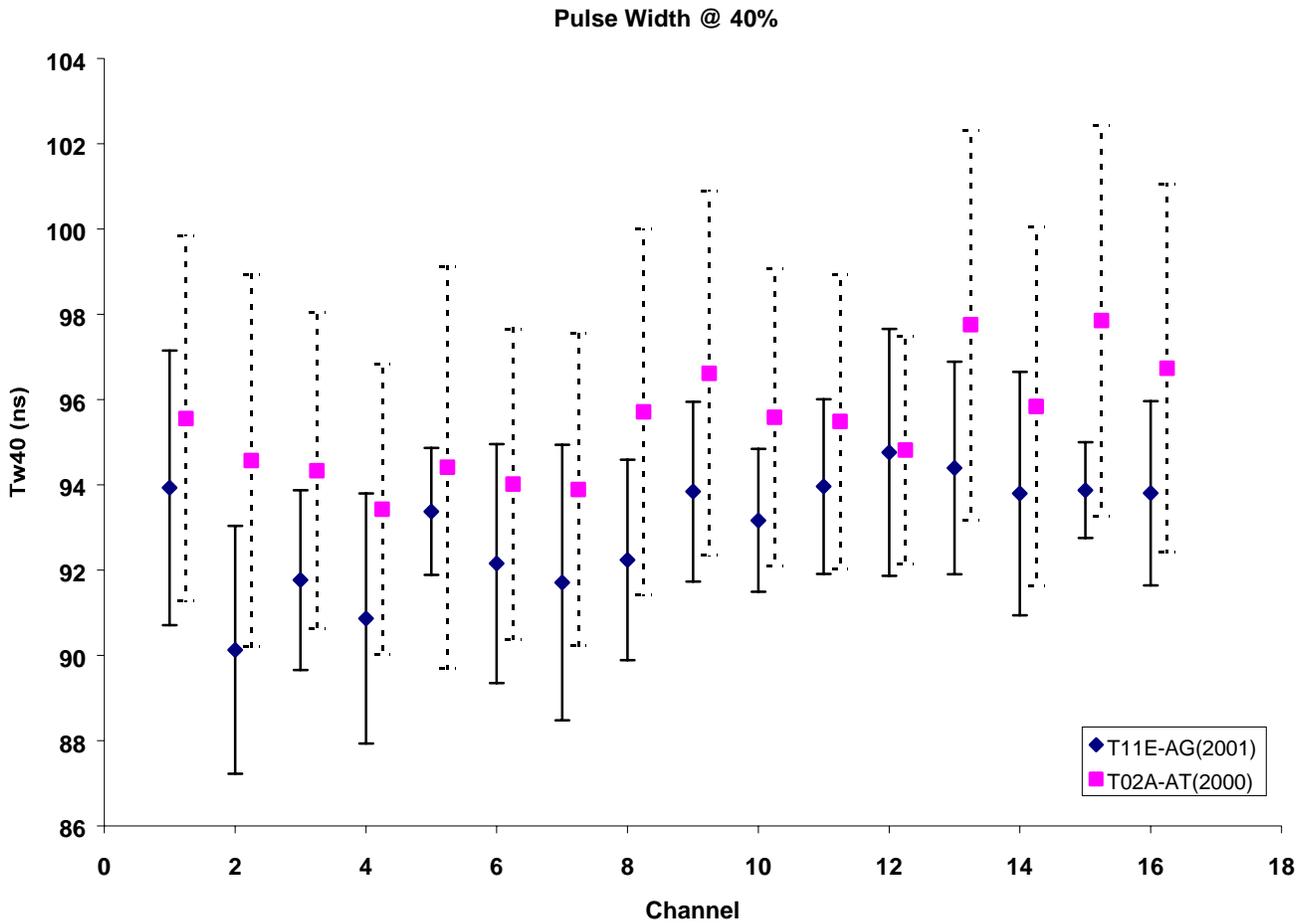
Worst case measured Standard Deviation channel to channel:

T11E-AG : 2.67%
T02A-AT : 5.57%



Pulse width at 40% of pulse height:

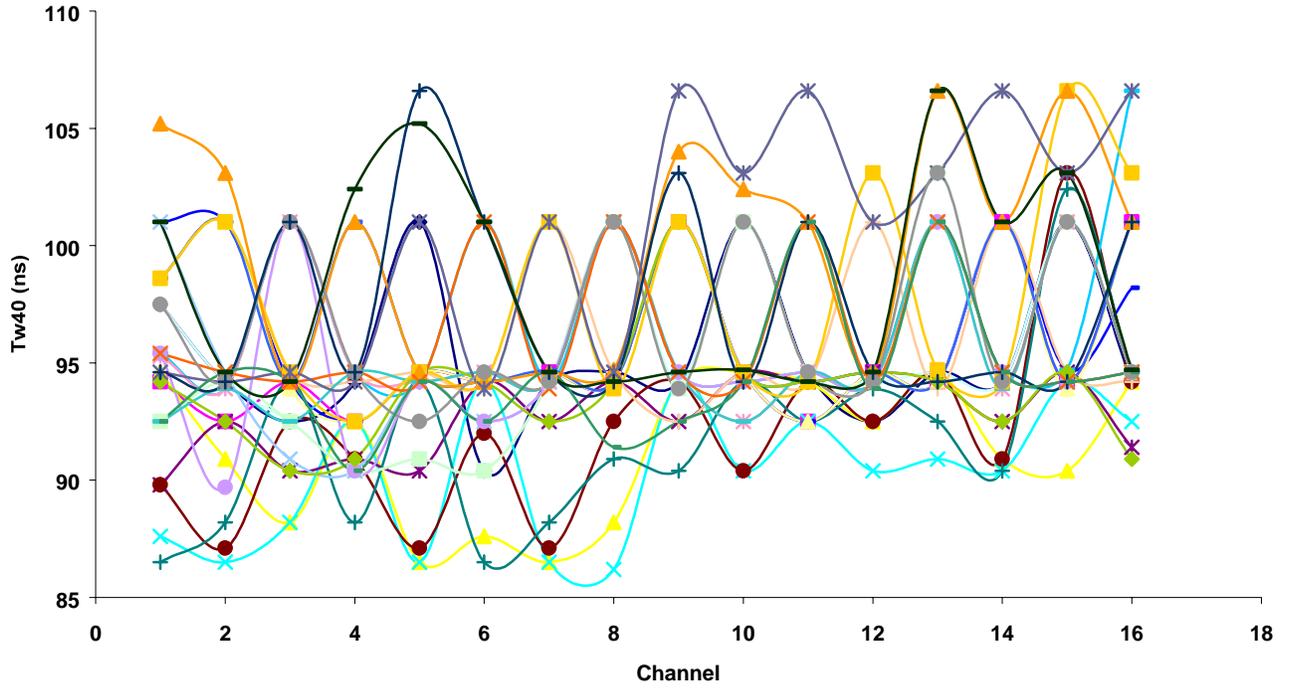
	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15	Ch16
T11E	93.93	90.13	91.77	90.87	93.38	92.16	91.71	92.24	93.84	93.17	93.96	94.76	94.40	93.80	93.88	93.81
	3.43%	3.22%	2.30%	3.23%	1.60%	3.04%	3.52%	2.55%	2.25%	1.80%	2.18%	3.06%	2.64%	3.05%	1.20%	2.30%
T02A	4.01	4.16	4.08	4.16	4.02	4.18	4.11	4.08	4.10	4.16	4.13	4.11	4.12	4.17	3.90	4.01
	4.48%	4.61%	3.93%	3.65%	4.98%	3.87%	3.90%	4.47%	4.42%	3.65%	3.62%	2.82%	4.67%	4.40%	4.68%	4.46%



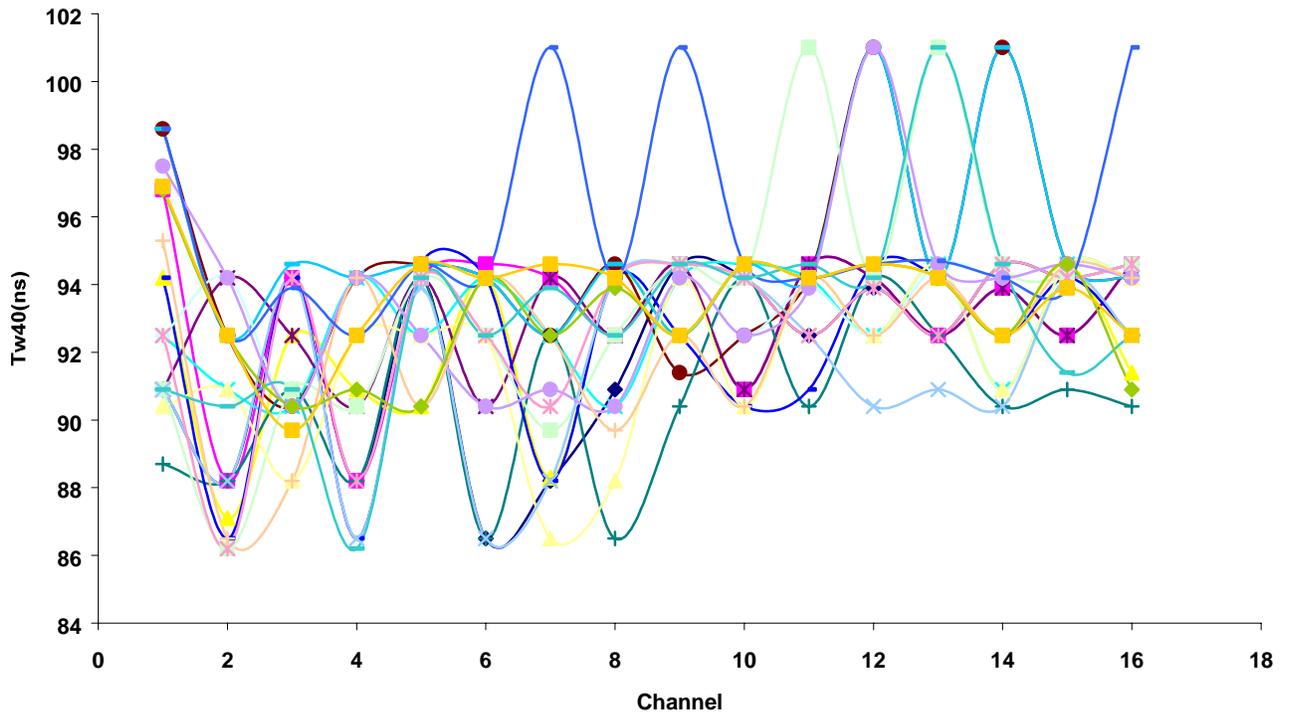
Worst case measured Standard Deviation channel to channel:

T11E-AG : 4.01%
 T02A-AT : 5.13%

Channel Dependency (T02A-AT)

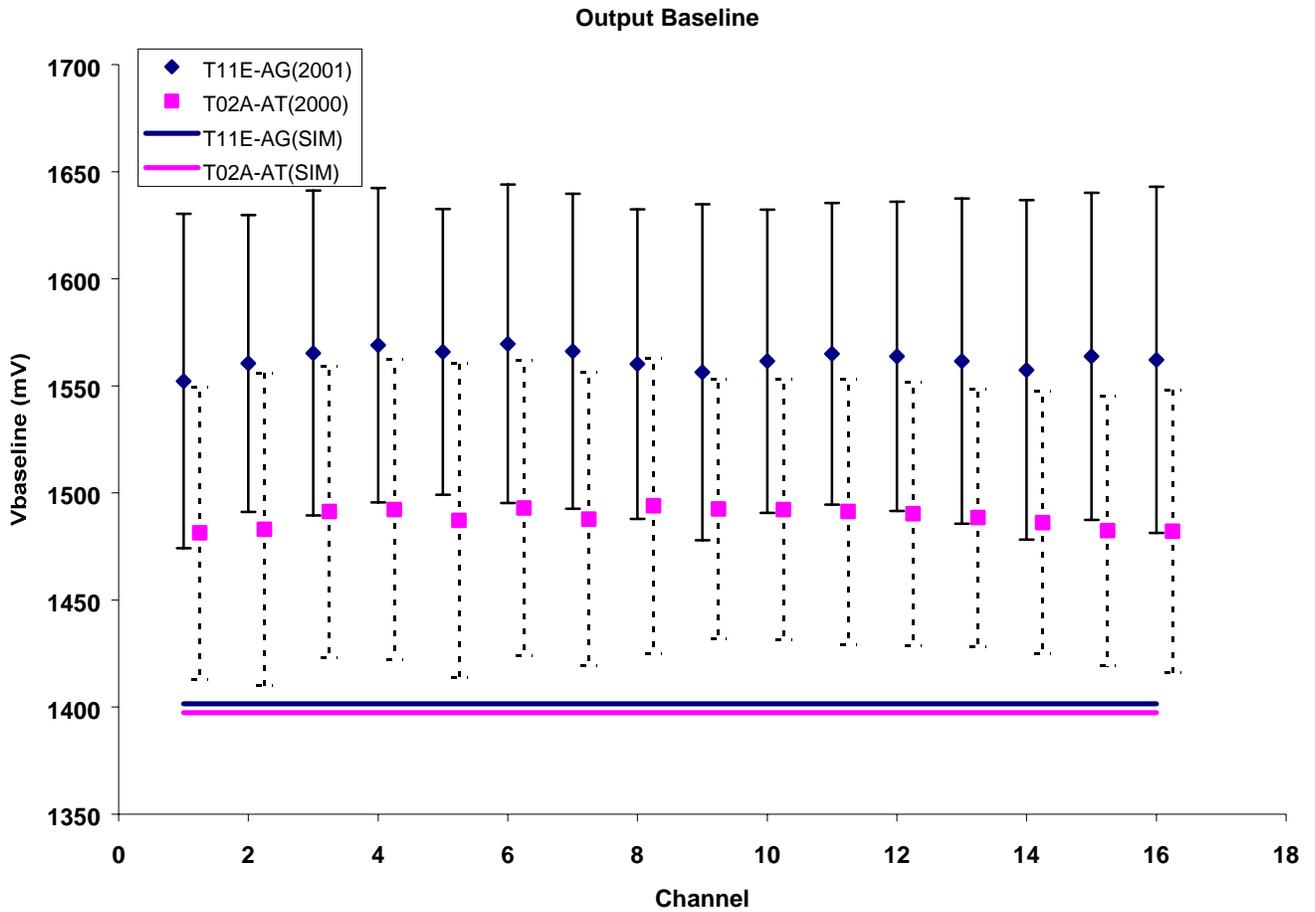


Channel Dependency (T11E-AG)



Output Baseline:

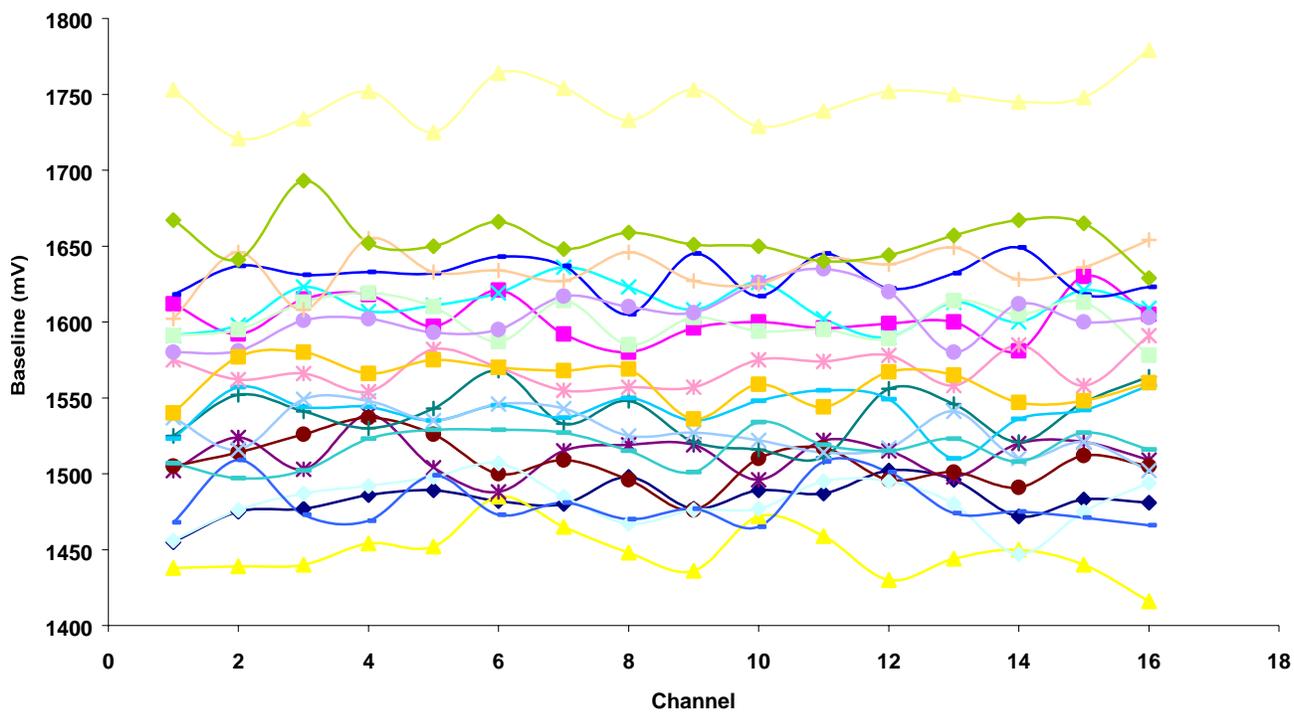
	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15	Ch16
T11E	1552.3	1560.5	1565.3	1569.0	1565.9	1569.6	1566.2	1560.2	1556.4	1561.5	1565.0	1563.8	1561.6	1557.5	1563.8	1562.1
	5.03%	4.44%	4.85%	4.67%	4.26%	4.74%	4.69%	4.63%	5.04%	4.54%	4.50%	4.61%	4.86%	5.08%	4.88%	5.17%
T02A	1481.3	1483.0	1491.3	1492.1	1487.1	1492.9	1487.7	1493.9	1492.4	1492.2	1491.3	1490.3	1488.5	1486.1	1482.3	1482.1
	4.61%	4.90%	4.57%	4.69%	4.93%	4.62%	4.60%	4.62%	4.07%	4.09%	4.16%	4.12%	4.04%	4.13%	4.25%	4.44%



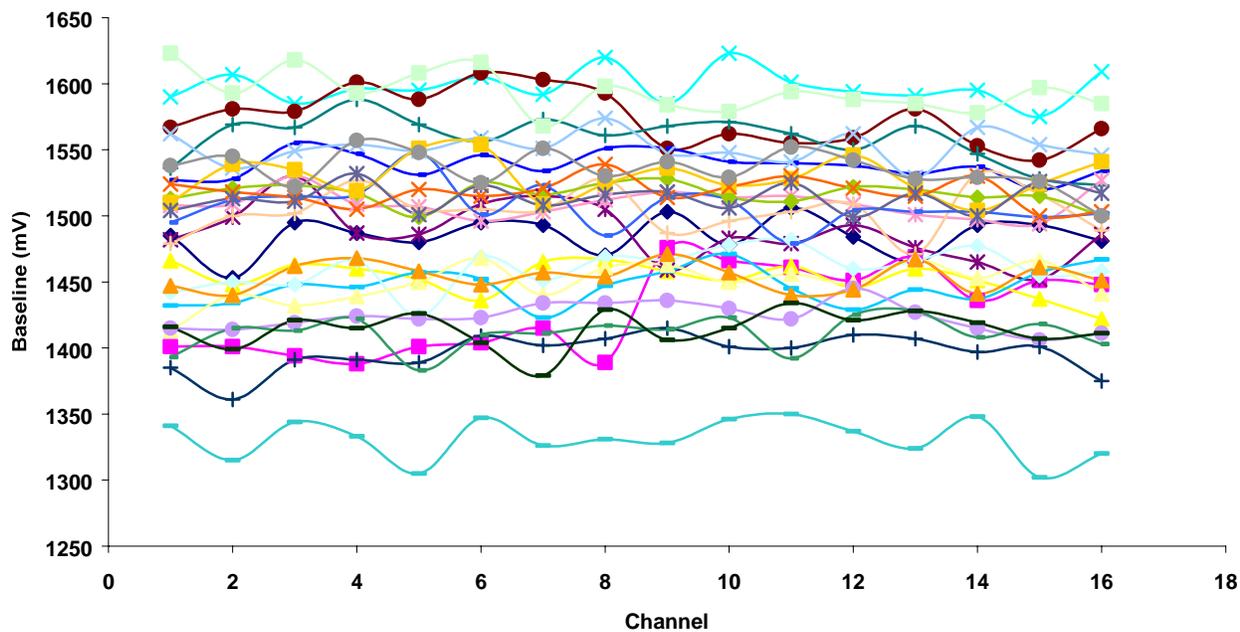
Worst case measured Standard Deviation channel to channel:

T11E-AG : 1.16%
 T02A-AT : 2.23%

Channel Dependency (T11E-AG)



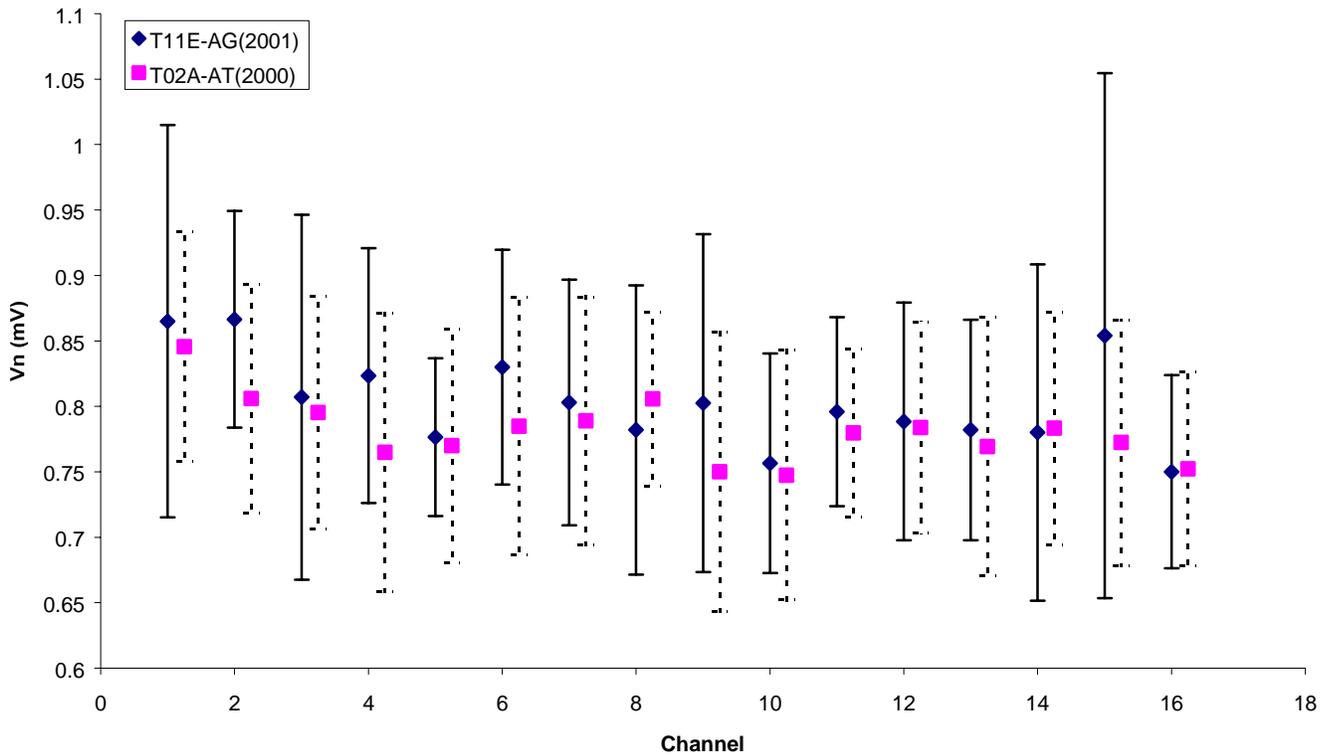
Channel Dependency (T02A-AT)



R.M.S Noise at the output (No detector capacitance):

	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15	Ch16
T11E	0.87	0.87	0.81	0.82	0.78	0.83	0.80	0.78	0.80	0.76	0.80	0.79	0.78	0.78	0.85	0.75
	17%	10%	17%	12%	8%	11%	12%	14%	16%	11%	9%	12%	11%	16%	23%	10%
T02A	0.85	0.81	0.80	0.76	0.77	0.78	0.79	0.81	0.75	0.75	0.78	0.78	0.77	0.78	0.77	0.75
	10%	11%	11%	14%	12%	13%	12%	8%	14%	13%	8%	10%	13%	11%	12%	10%

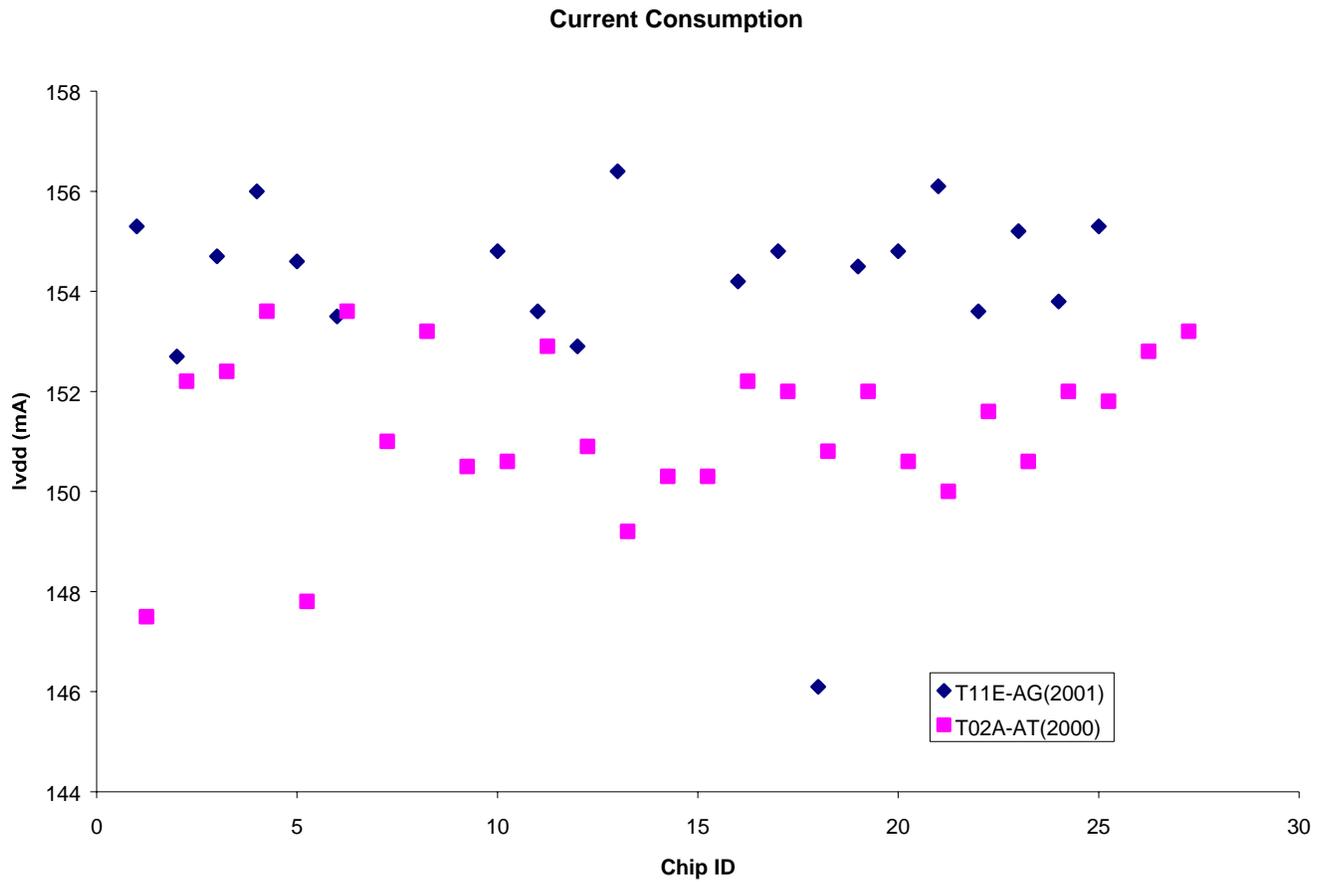
R.M.S Noise @ output



Worst case measured Standard Deviation channel to channel:

T11E-AG : 24.2%
 T02A-AT : 16.1%

Power :



In lot Chip to Chip variation:

Lot T11E-AG : 1.39% (mean: 154.1mA)

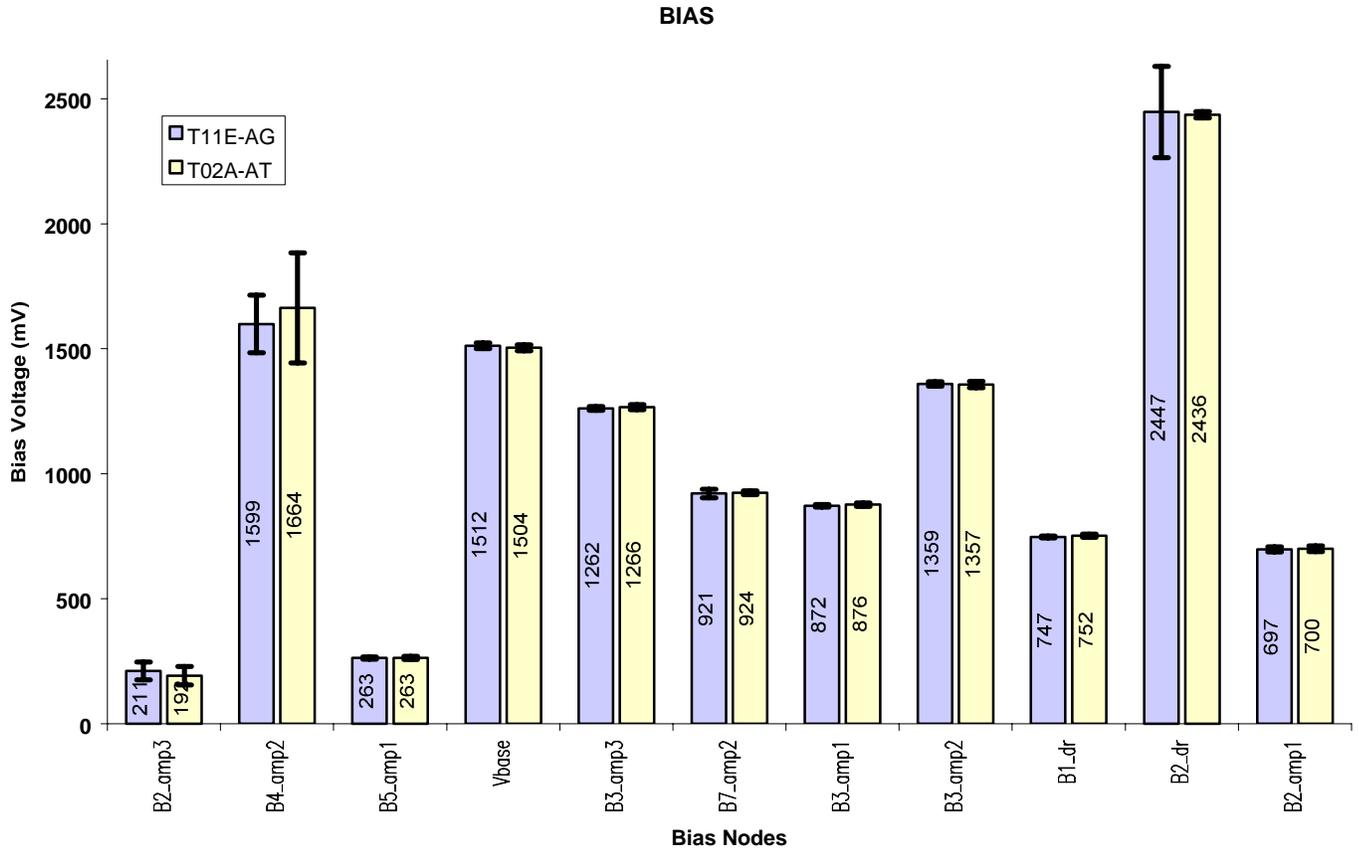
Lot T02A-AT: 1.04% (mean: 151.3mA)

Lot to Lot Variation:

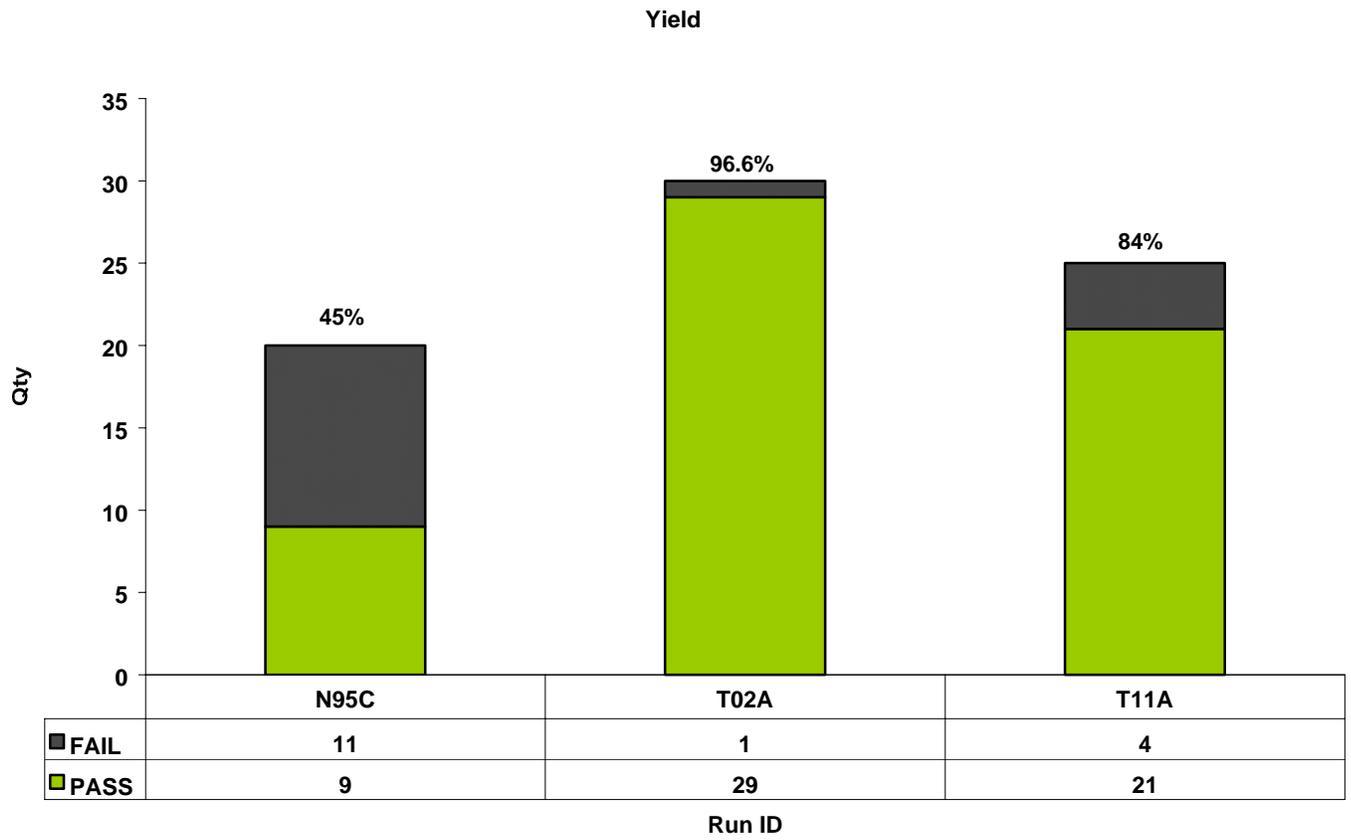
1.51% (mean: 152.5mA)

Bias Voltages:

	B2_amp3	B4_amp2	B5_amp1	Vbase	B3_amp3	B7_amp2	B3_amp1	B3_amp2	B1_dr	B2_dr	B2_amp1
T11E	211.45	1599.05	262.85	1512.45	1261.5	920.85	871.65	1359.25	747.3	2447.1	697.05
	16.92%	7.18%	1.89%	0.75%	0.63%	1.92%	0.58%	0.63%	0.56%	7.46%	1.45%
T02A	191.85	1663.52	263.30	1504.15	1266.33	924.26	876.41	1356.59	752.22	2435.89	699.96
	19.2%	13.2%	2.5%	0.8%	0.8%	0.8%	0.8%	0.9%	0.8%	0.5%	1.7%



Yield:



Cumulative yield : 78.8%

Failure modes:

BIAS	Failures		Cbias	Cbias_ext	Cbias_total	TYPE
b2_amp1	4	VDD	100	95	195	2P
b2_amp3	3	VDD	17	85	102	1N
b2_dr	3	VDD	30	85	115	1P
b7_amp3	2	GND	17	50	67	1P
b1_dcs	2	GND	22	125	147	1P
b3_amp1	2	GND	30	50	80	1P
b3_amp3	2	GND	17	125	142	1P
b5_amp1	2	VDD	100	85	185	2P
b5_amp2	1	VDD	10	85	95	1P
b5_amp3	1	VDD	10	125	135	1N
b1_dr	1	GND	29	50	79	1P
b4_amp2	1	VDD	15	50	65	1N
b3_amp2	0	GND	15	50	65	1P
b1_rst	0	GND	10	16	26	-
b4_amp1	0	GND		95	95	-
b7_amp2	0	GND	10	50	60	1P
vbase	0	GND	46	50	96	1P

Total Bias failures: 24 (15 bypassed to VDD and 9 bypassed to GND)

Type:

- 1 : Startup
- 2 : Standard
- 1P: Pmos Threshold ref.
- 1N: Nmos Threshold ref.

CSC Electronics Noise Measurement

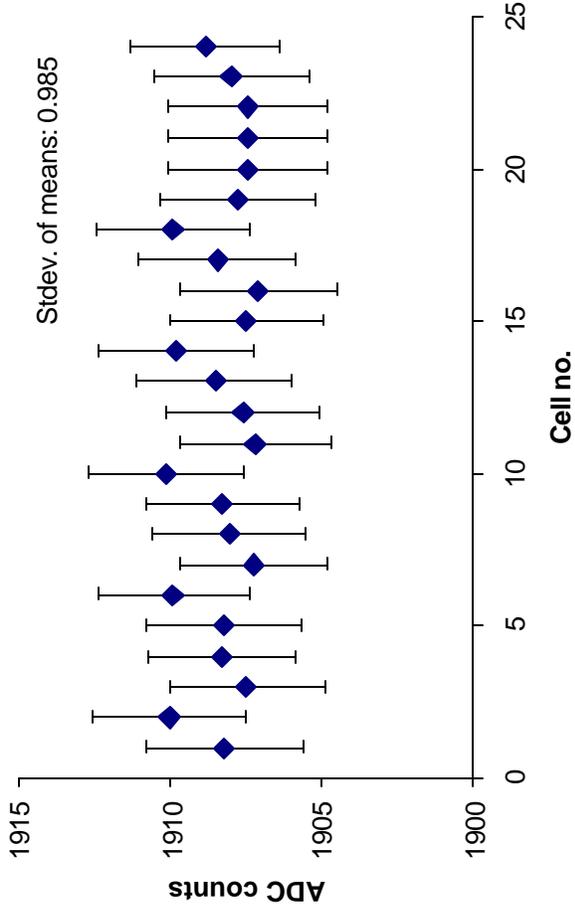
IC50 preamp/shaper (unpulsed) into SCA on ASM-IIa board

Channel 1 results displayed

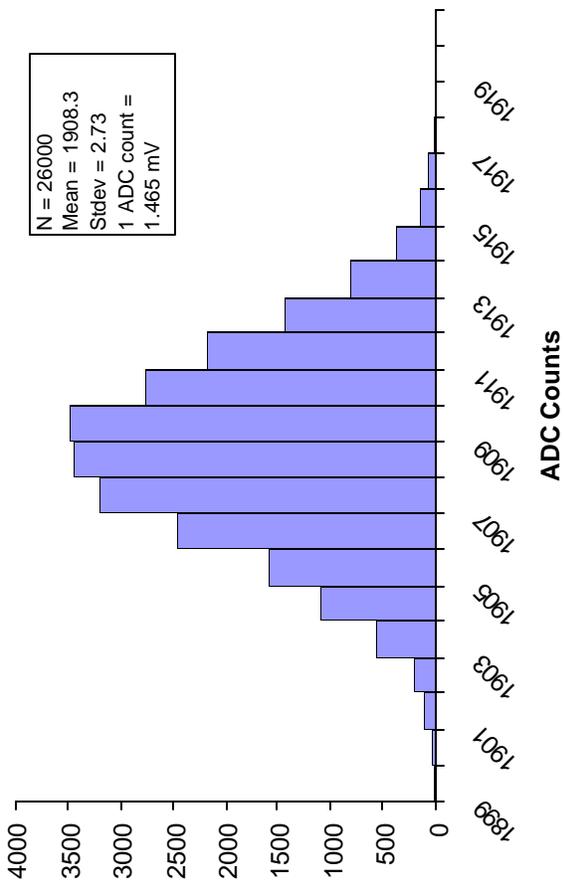
24 SCA cells written and read out

Measurement repeated for 1000 cycles.

Mean and s.d. of each cell



Histogram of all cells



A

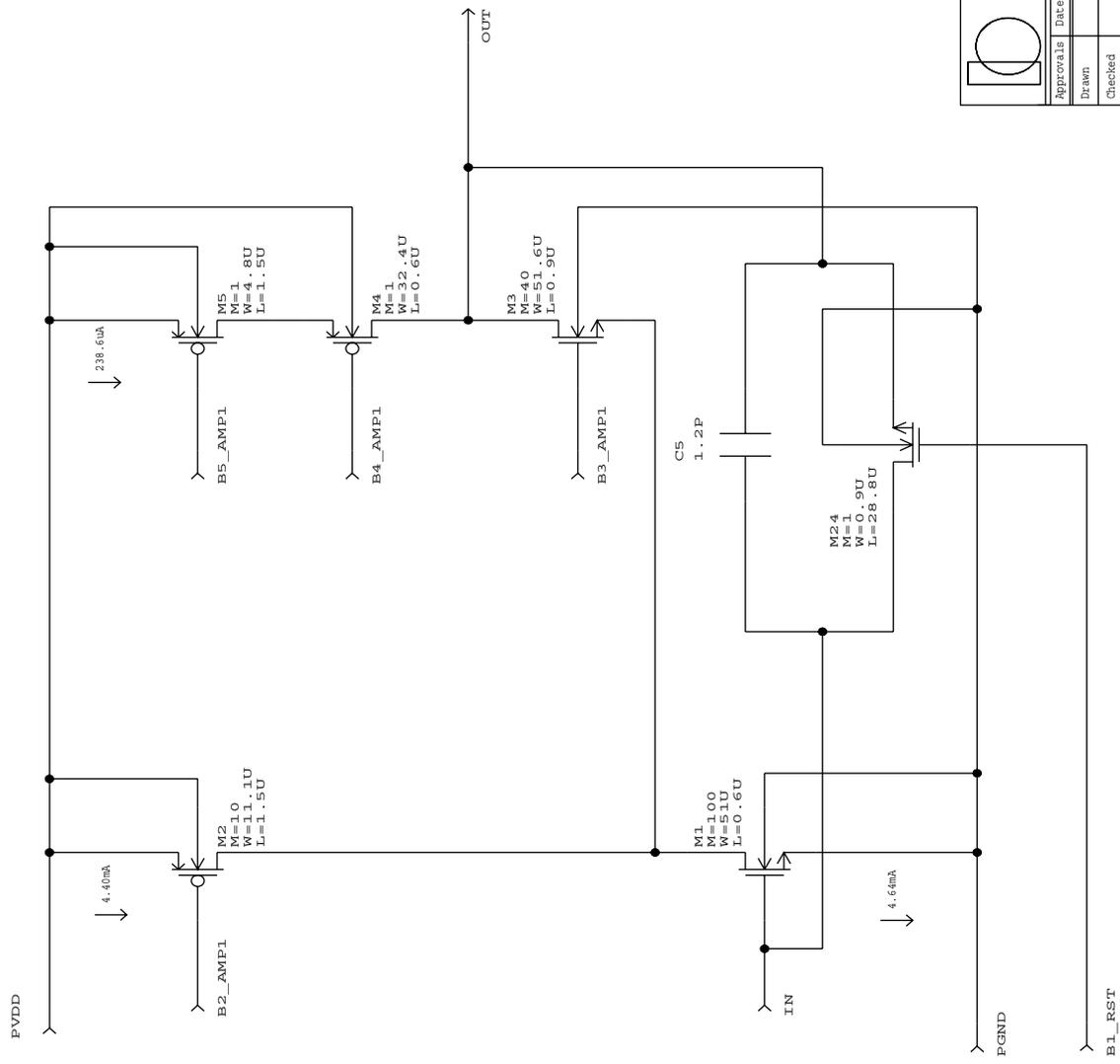
B

C

D

Bias lines:
 B1_BST
 B2_P
 B3_P
 B4_P**
 B5_P

PVDD: 3.3V
 PGND: 0V
 Rf: 1M
 Pdiss: 15mW



Notes:

** BIAS line B4_P is grounded off chip**
 Changed M3 [M=10,W=206.7U] to [M=40,W=51.6U]

Approvals	Date	Drawings
Drawn		
Checked		
Issued		

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ATLAS CSC / HP CMOS14TB 0.5U
 PREAMP

IC50

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 anandk@bnl.gov

Sheet: 1 of 1

A

B

C

D

Bias lines:
 B3_AMP2
 B4_AMP2
 B5_AMP2
 B7_AMP2

AVDD: 3.3V
 AGND: 0V
 Pdiss: 2.9mW

Notes:
 Changed the Following:
 M1 W=32U to W=32.1U
 M3 W=22U to 21.9U
 M5 W=31U to 30.9U



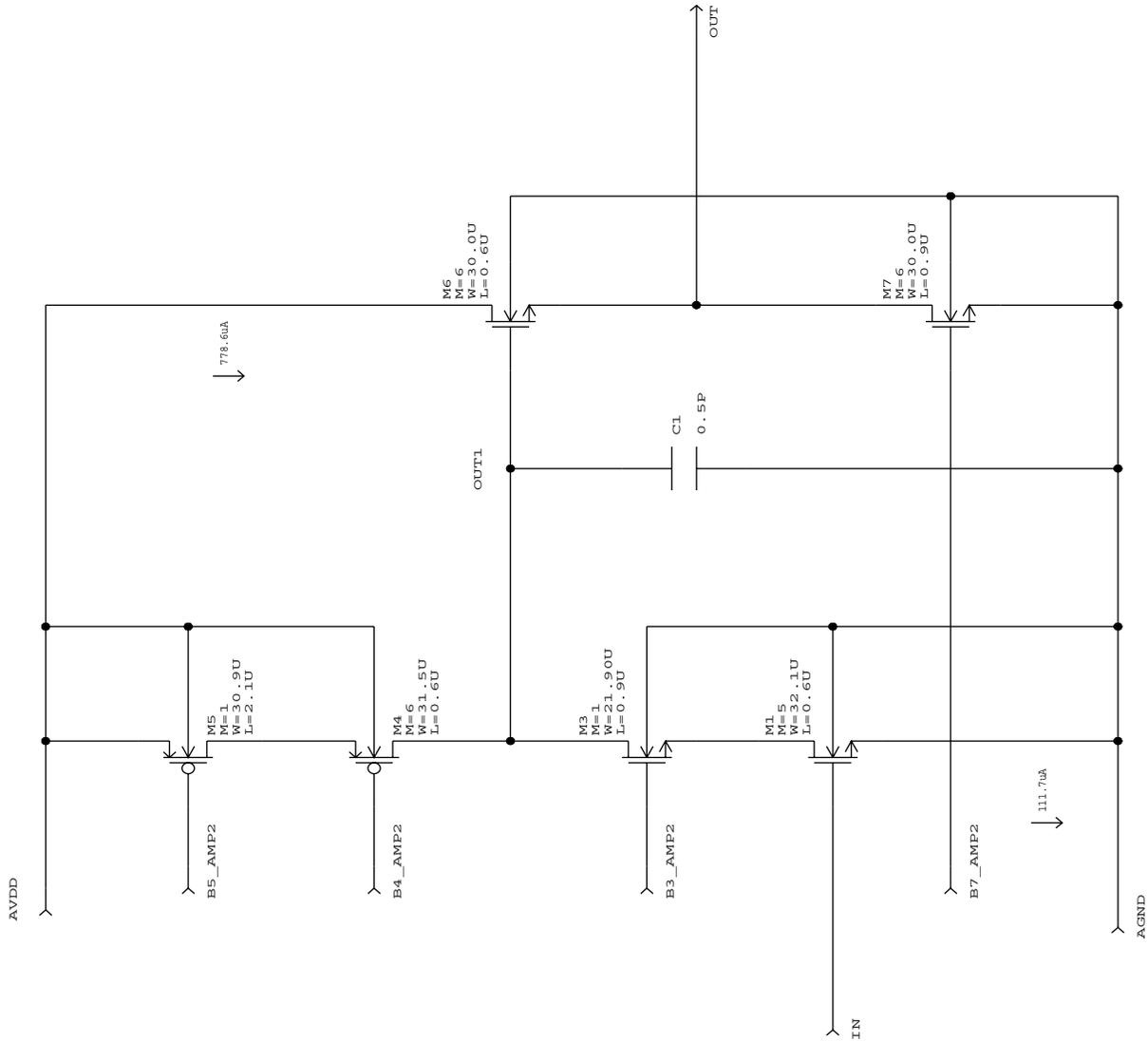
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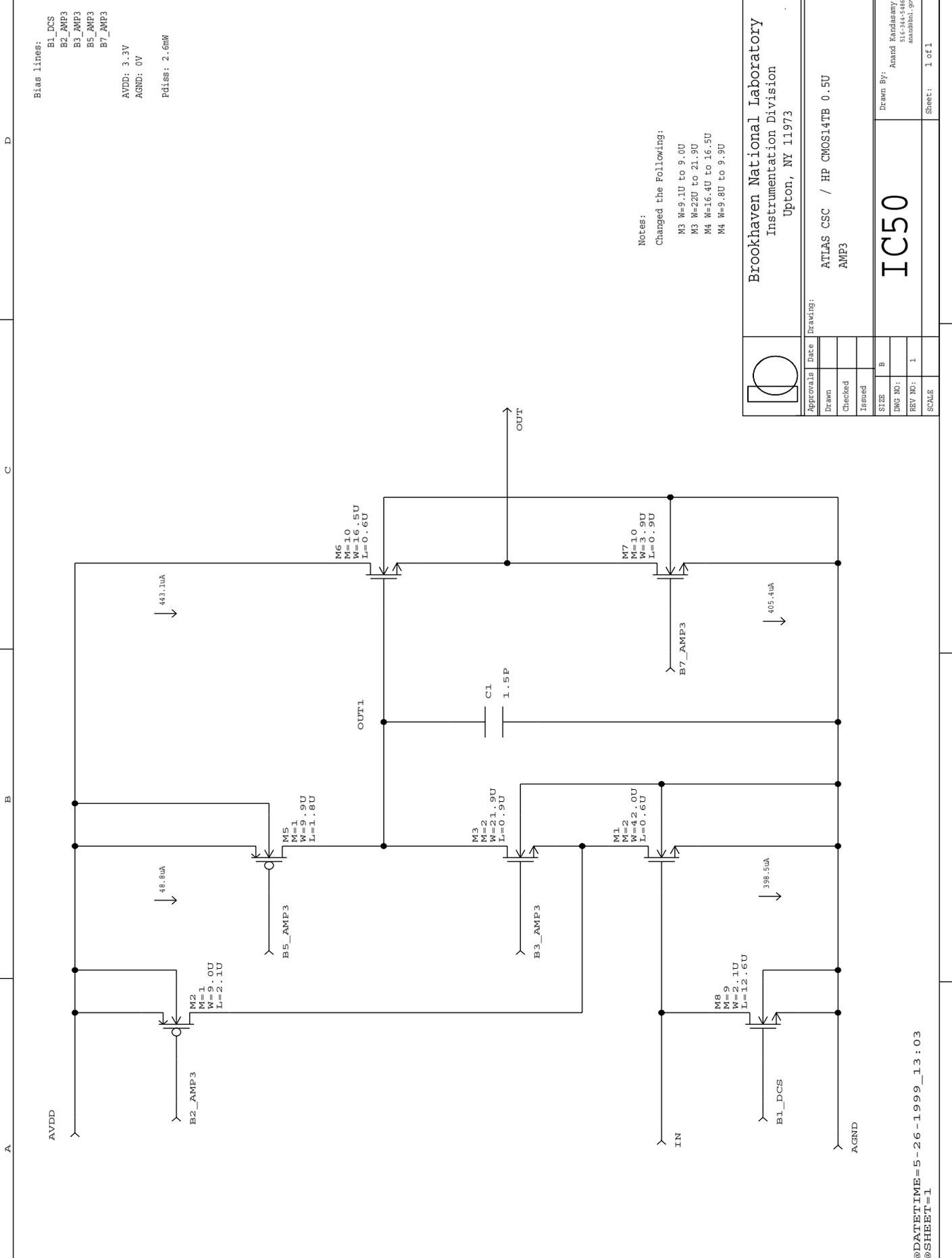
Approvals | Date | Drawings:

ATLAS CSC / HP CMOS14TB 0.5U
 AMP2

IC50

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 Sheet: 1 of 1





Bias lines:
 B1_DCS
 B2_AMP3
 B3_AMP3
 B5_AMP3
 B7_AMP3

AVDD: 3.3V
 AGND: 0V
 Pdiss: 2.6mW

Notes:
 Changed the Following:
 M3 W=9.1U to 9.0U
 M3 W=22U to 21.9U
 M4 W=16.4U to 16.5U
 M4 W=9.8U to 9.9U

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ATLAS CSC / HP CMOS14TE 0.5U
 AMP3

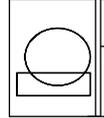
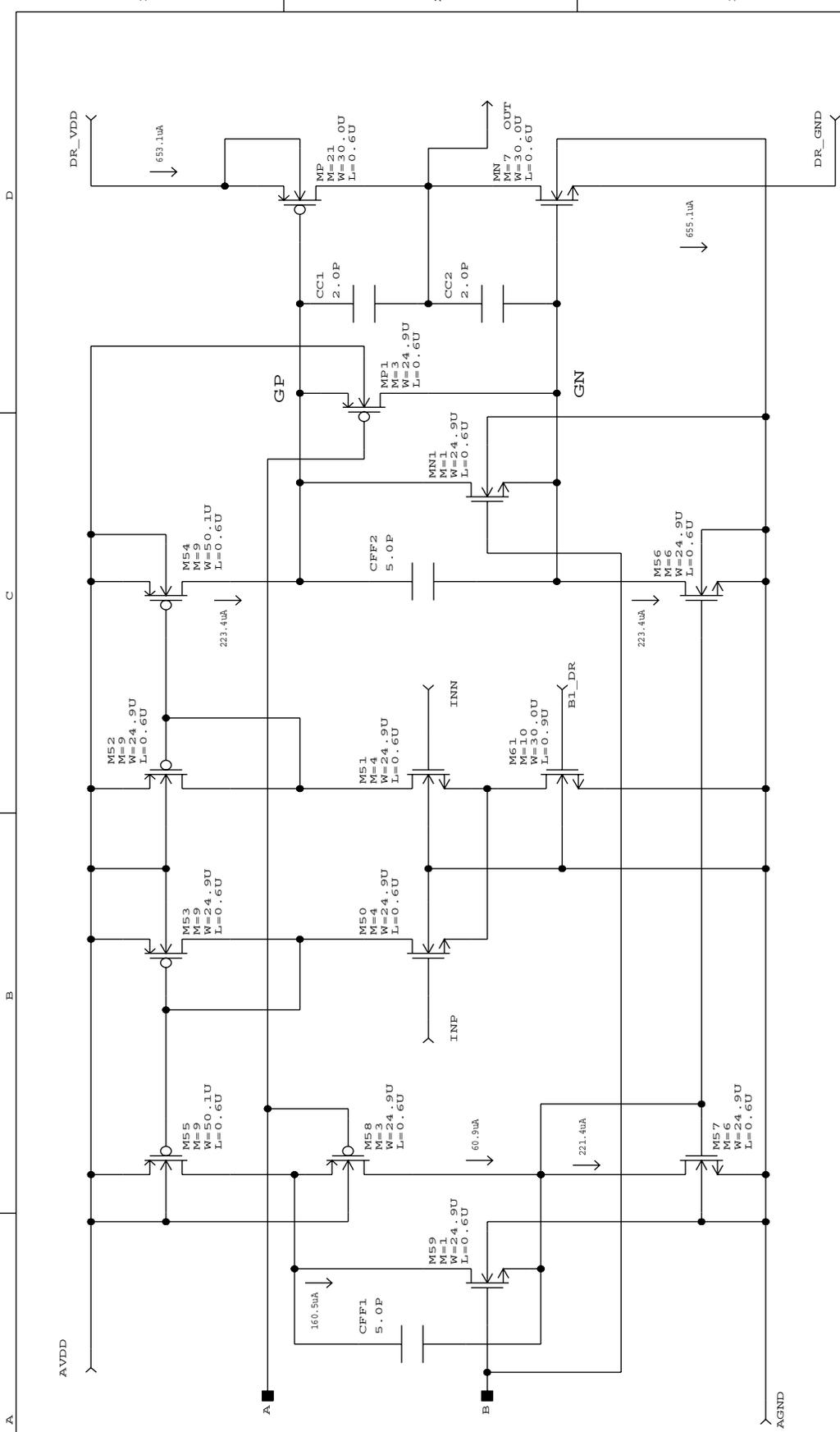
IC50

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Sheet: 1 of 1

Drawings:

Approvals	Date
Drawn	
Checked	
Issued	
SIZE	B
DWG NO:	
REV NO:	1
SCALE	



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Approvals	Date	Drawn by
Drawn		
Checked		
Issued		

ATLAS CSC / HP CMOS14TB 0.5U
CLASS AB DRIVER

IC50

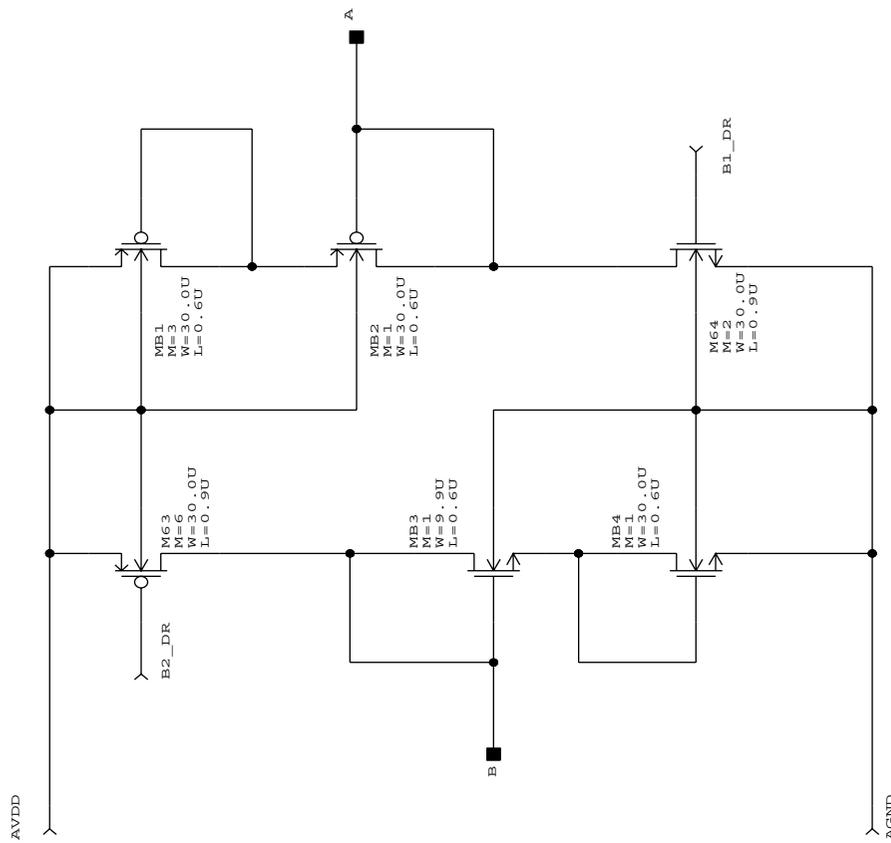
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anandk@bnl.gov
Sheet: 1 of 2

Bias lines:
A
B
B1_DR
B2_DR

AVDD/DR_VDD: 3.3V
GND/DR_GND: 0V

Pdiss: 4.5mW

Notes:
Changed the Following:
M50, M51, M52, M53, M56, M57, M58, M59, MP1 and MN1 W=25U to 24.9U
M54 and M55 W=50U to 50.1U



Bias lines:
 A
 B
 B1_DR
 B2_DR

AVDD/DR_VDD: 3.3V
 GND/DR_GND: 0V
 Pdiss: 4.5mW

Notes:
 Changed the Following:
 MB3 W=10.0U to 9.9U



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Checked	
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ATLAS CSC CLASS AB DRIVER / HP CMOS14TB 0.5U
 CLASS AB DRIVER

IC50

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Sheet: 1 of 2

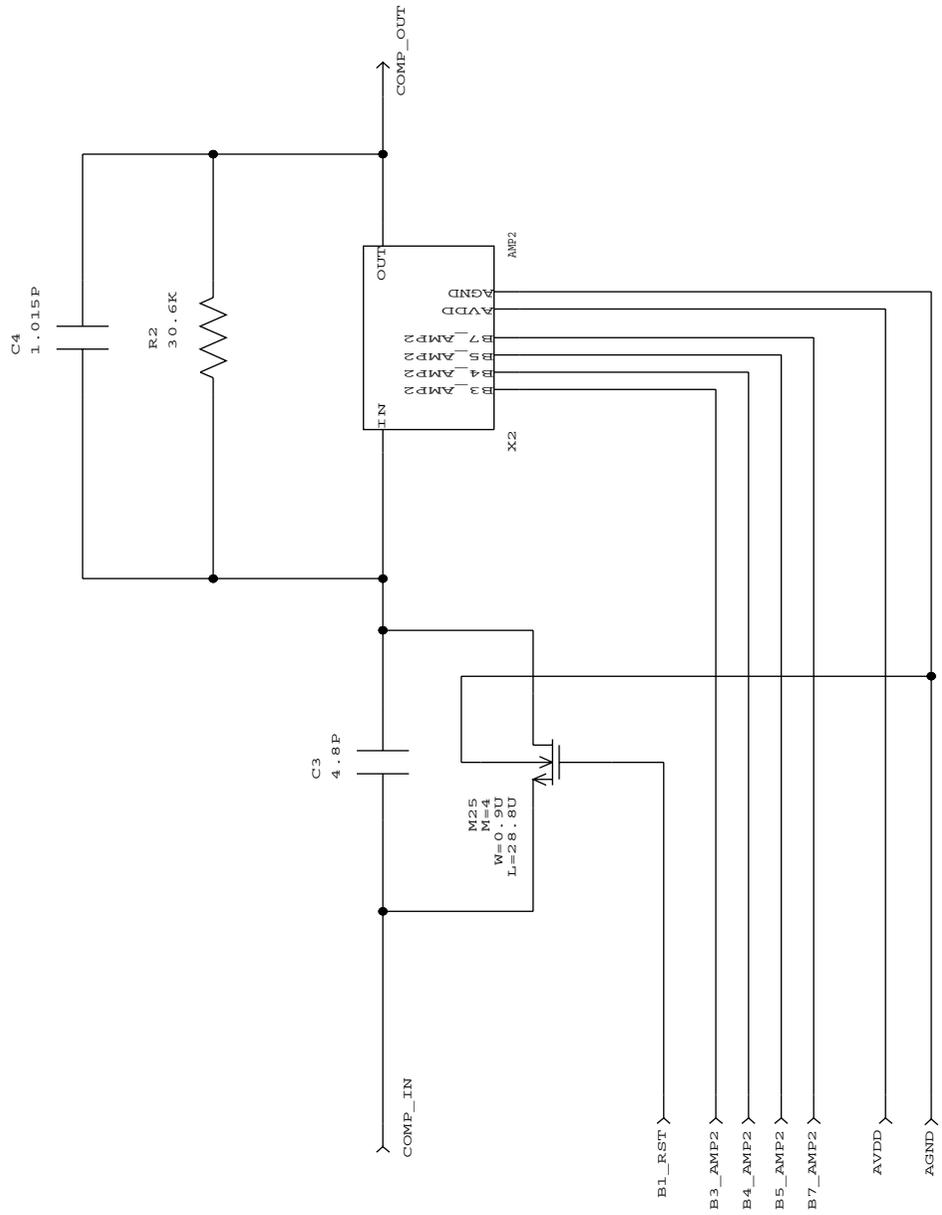
A

B

C

D

Bias lines:
 B1_RST
 B3_AMP2
 B4_AMP2
 B5_AMP2
 B7_AMP2
 AVDD: 3.3V
 AGND: 0V



Notes:

M25 : Four copied of M24 (Feedback FET of PREAMP) - Layout

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ATLAS CSC / HP CMOS14TB 0.5U
 COMPENSATION

IC50

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 Sheet: 1 of 1

1

2

3

4

A

B

C

D

A

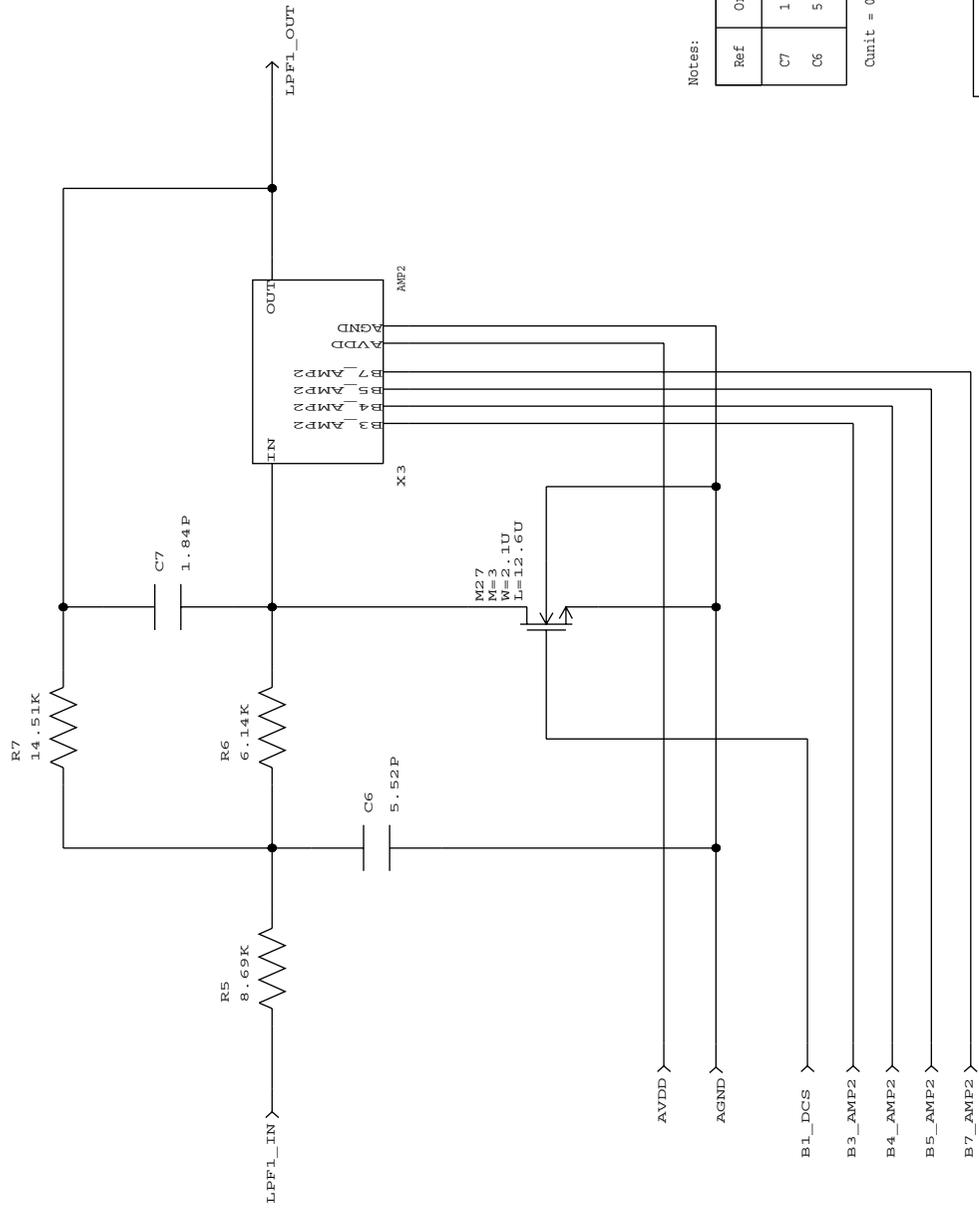
B

C

D

SEE NOTES ON THESE VALUES

Bias lines:
 B3_AMP2
 B4_AMP2
 B5_AMP2
 B7_AMP2
 B1_DCS
 AVDD: 3.3V
 AGND: 0V



M27
 M=3
 W=2.1U
 L=12.6U

Notes:

Ref	Original	Changed	Copies	Error	Ratio
C7	1.88P	1.84P	Unit*2	-	-
C6	5.52P	5.52P	Unit*6	2.2%	C6/C7 = 2.936

Unit = 0.92P

Approvals	Date	Drawn by:
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ATLAS CSC / HP CMOS14TB 0.5U
 Low Pass Filter Stage 1

IC50

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 Sheet: 1 of 1

1

2

3

4

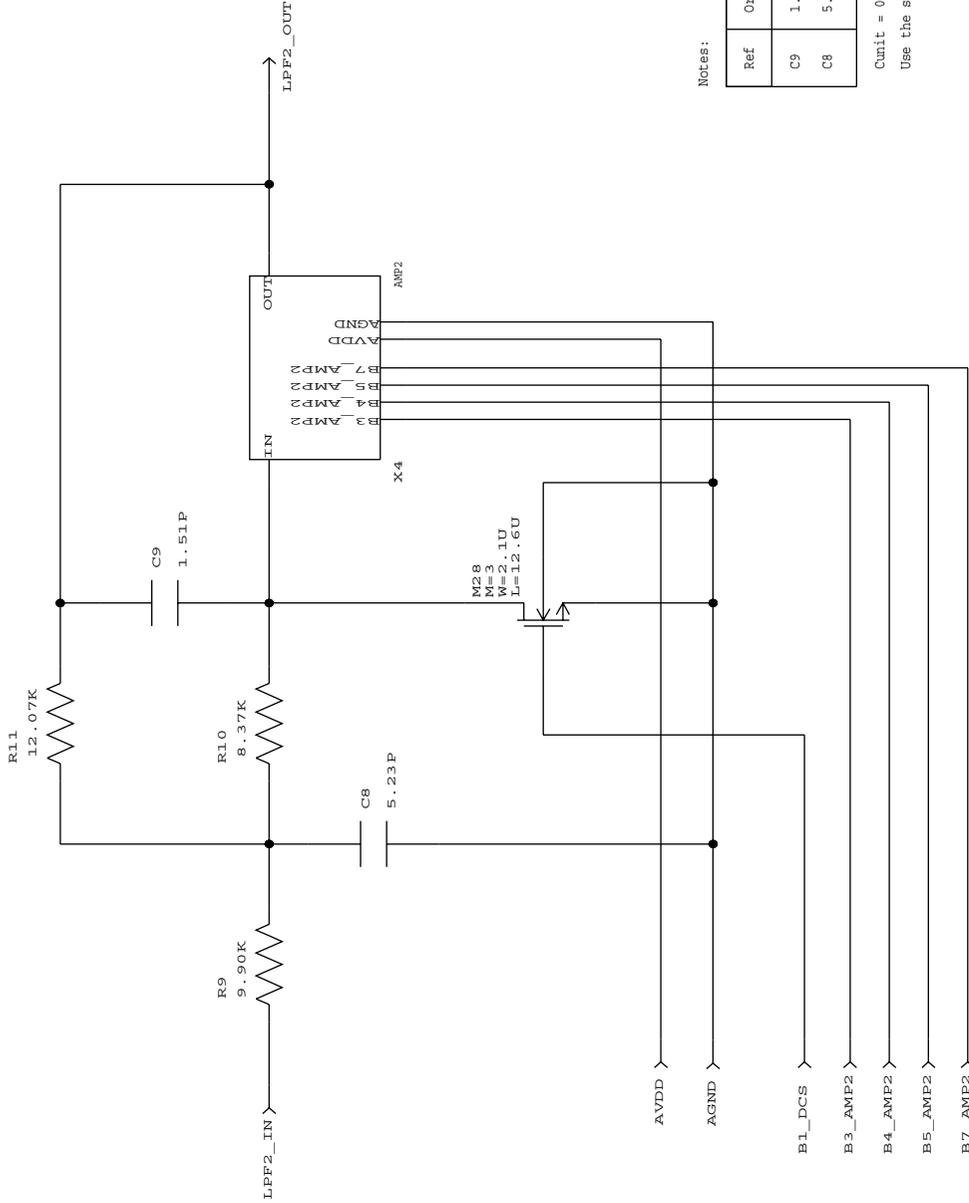
A

B

C

D

SEE NOTES ON THESE VALUES



Bias lines:
 B3_AMP2
 B4_AMP2
 B5_AMP2
 B7_AMP2
 B1_DCS
 AVDD: 3.3V
 AGND: 0V

Notes:

Ref	Original	Changed	Copies	Error	Ratio
C9	1.51P	1.51P	Cunit*2	-	-
C8	5.23P	5.25P	Cunit*7	1%	C8/C9 = 3.463

Cunit = 0.75P
 Use the same Unit Capacitance in BP stage also



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ATLAS CSC / HP CMOS14TB 0.5U
 Low Pass Filter Stage 2

IC50

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 Sheet: 1 of 1

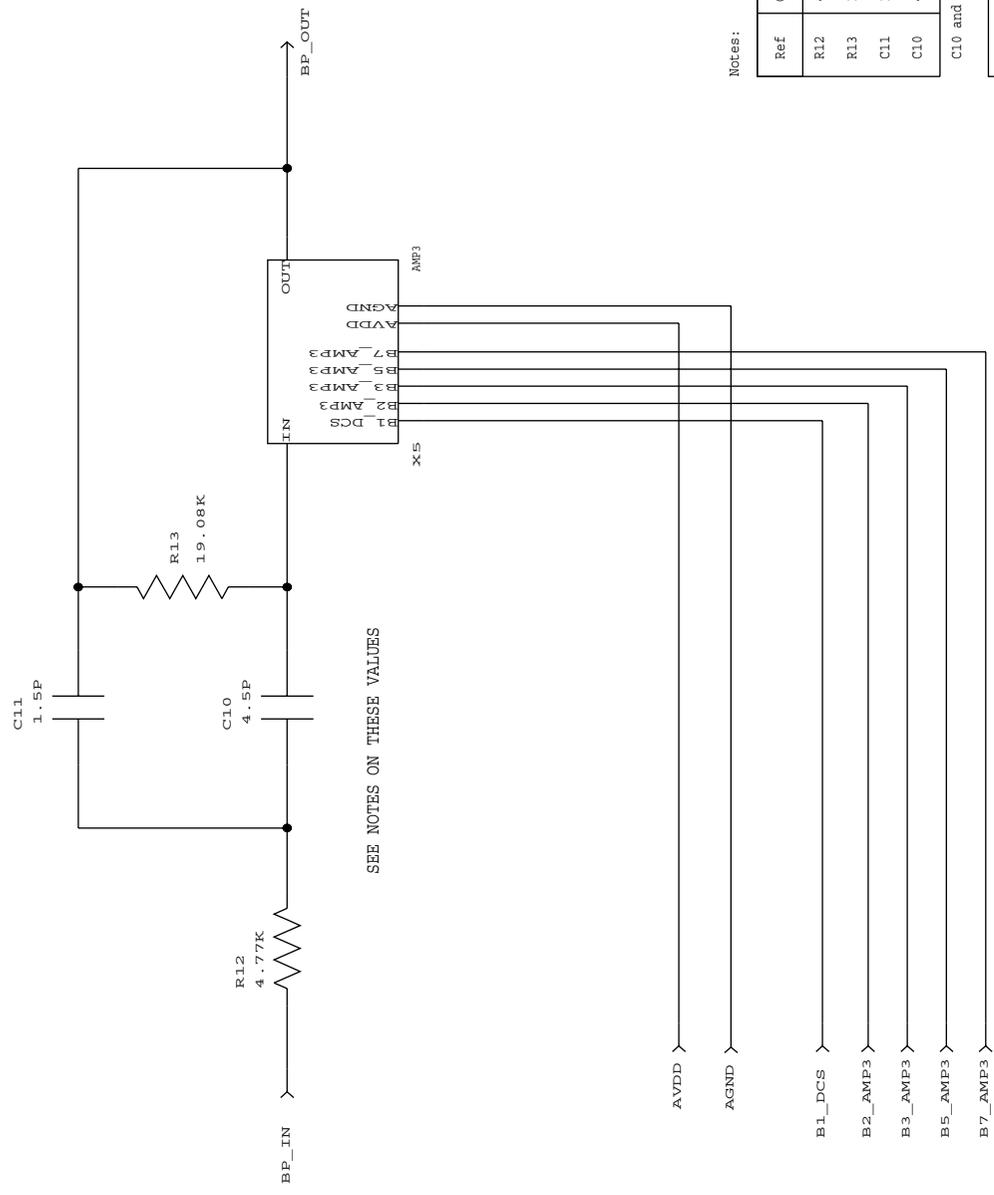
A

B

C

D

Bias lines:
 B2_AMP3
 B3_AMP3
 B5_AMP3
 B7_AMP3
 B1_DCS
 AVDD: 3.3V
 AGND: 0V

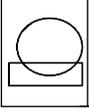


SEE NOTES ON THESE VALUES

Notes:

Ref	Original	Changed	Copies	Error	Ratio
R12	4.77K	4.77K	R12*1	-	-
R13	18.93K	19.08K	R12*4	0.8%	R13/R12 = 3.968
C11	1.46P	1.5P	C11*1	-	-
C10	4.53P	4.5P	C11*3	3.4%	C10/C11 = 3.102

C10 and C11 : Use Unit capacitance of 0.75P used in LP2 C9 and C8



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ATLAS CSC / HP CMOS14TB 0.5U
 Band Pass Filter

IC50

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 Sheet: 1 of 1

A

B

C

D

A

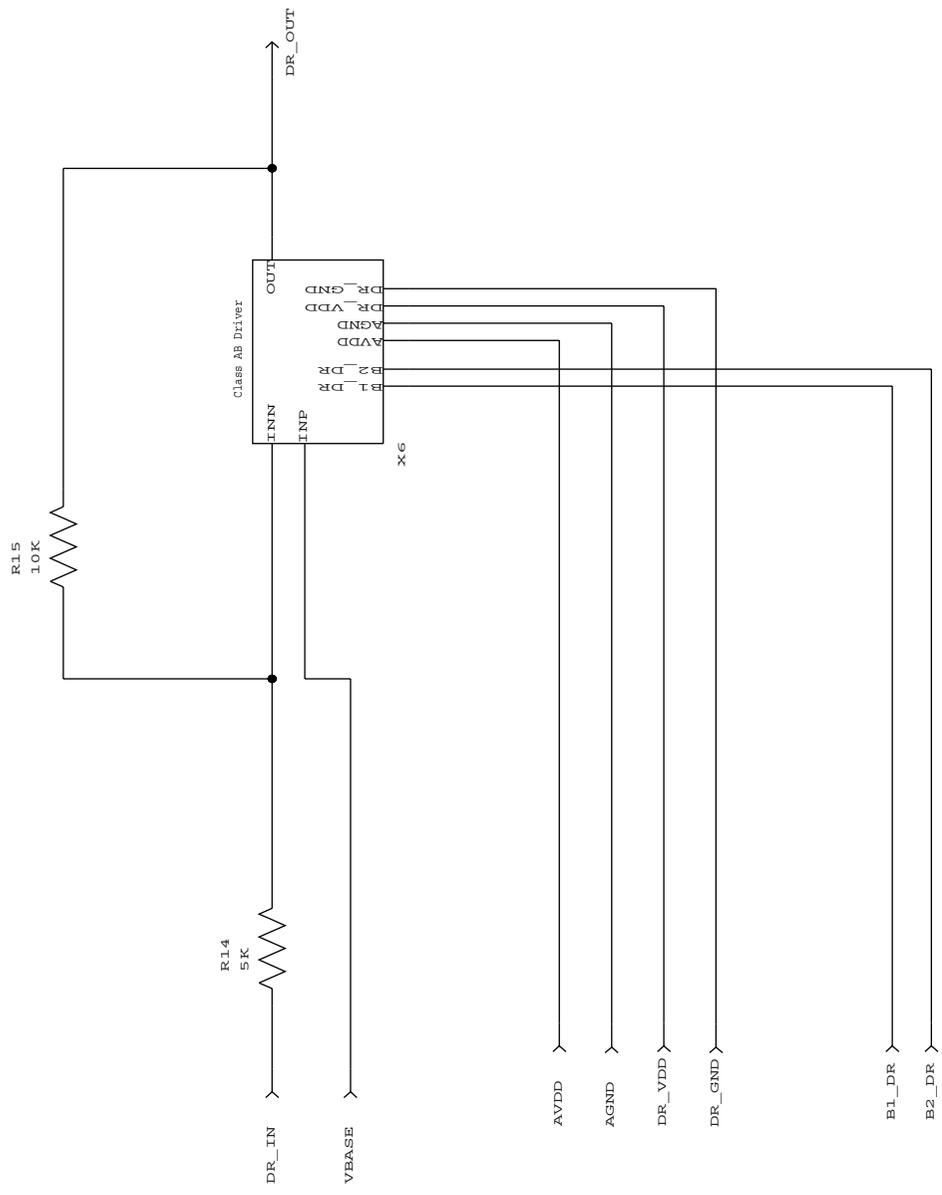
B

C

D

Bias lines:
 A
 B
 B1_DR
 B2_DR

AVDD/DR_VDD: 3.3V
 AGND/DR_GND: 0V



Notes:
 R1.5 = Two R1.4's in Series (Layout)



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ATLAS CSC / HP CMOS14TB 0.5U
 OUTPUT DRIVE STAGE

IC50

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Sheet: 1 of 1

1

2

3

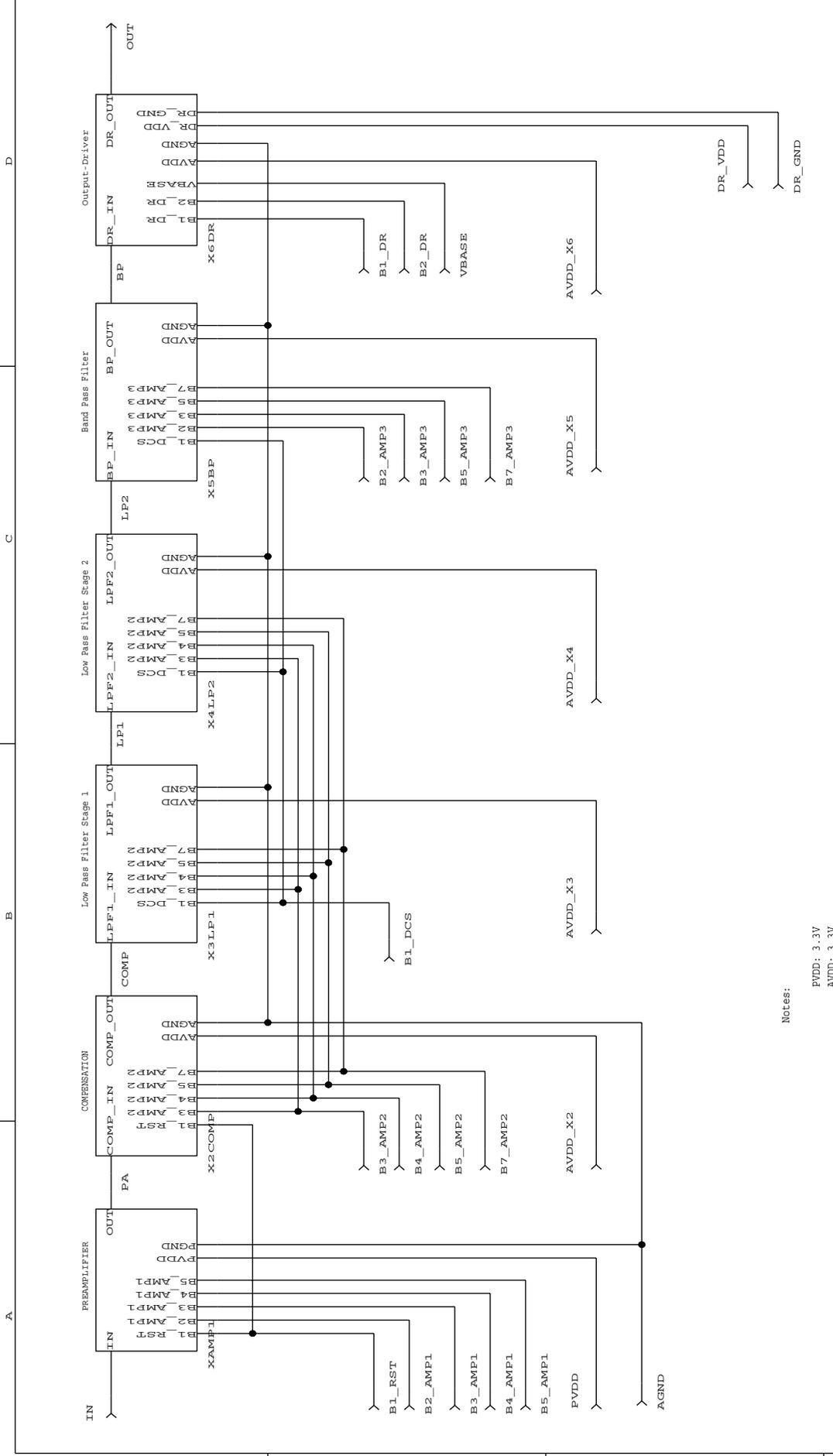
4

A

B

C

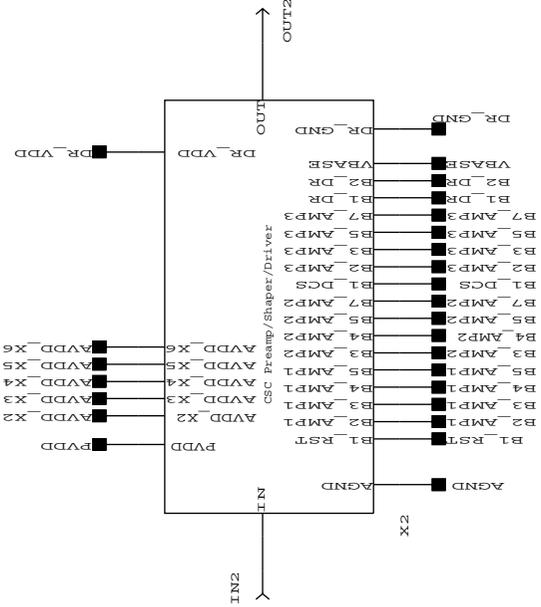
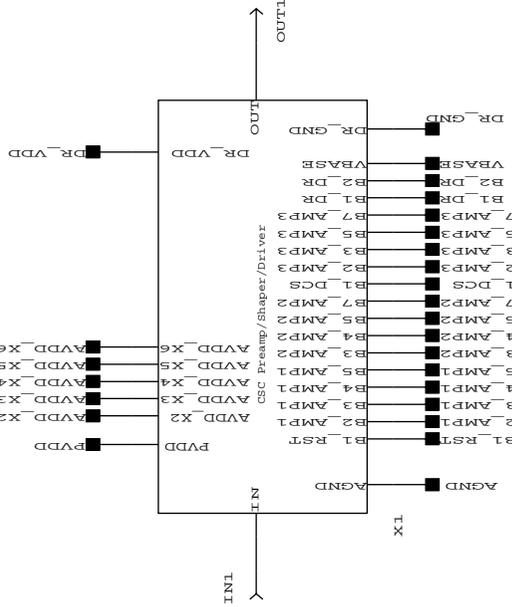
D



Notes:

- PVDD: 3.3V
- AVDD: 3.3V
- DR_VDD: 3.3V
- FGND: 0V
- DR_GND: 0V

	Brookhaven National Laboratory Instrumentation Division Upton, NY 11973	
	ATLAS CSC / HP CMOS14TB 0.5U CSC Preamp/Shaper Channel	<h1 style="font-size: 2em; margin: 0;">IC50</h1>
Drawn By: Anand Kandasamy Checked By: Anand Kandasamy Issue No: 1	Drawn By: Anand Kandasamy Checked By: Anand Kandasamy Issue No: 1	
SCALE	Sheet: 1 of 1	



Notes:

- P_VDD: 3.3V
- A_VDD: 3.3V
- DR_VDD: 3.3V
- A_GND: 0V
- DR_GND: 0V



Approvals Date Drawings:

Approvals	Date	Drawings
Drawn		
Checked		
Issued		

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

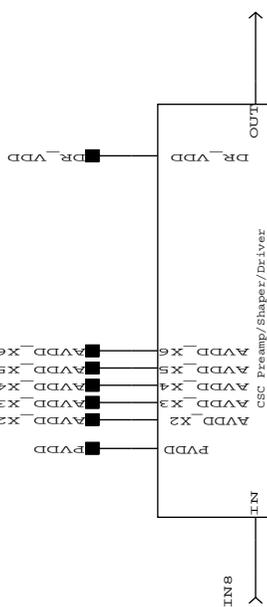
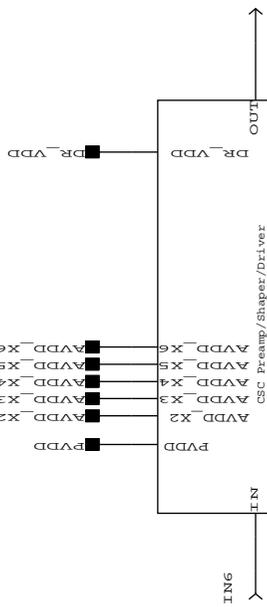
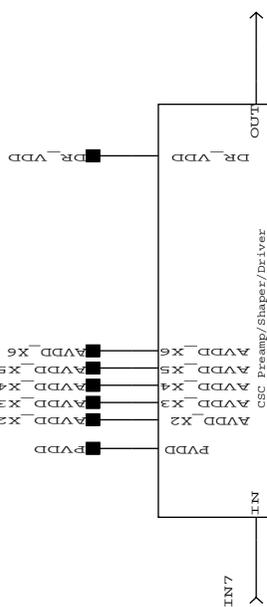
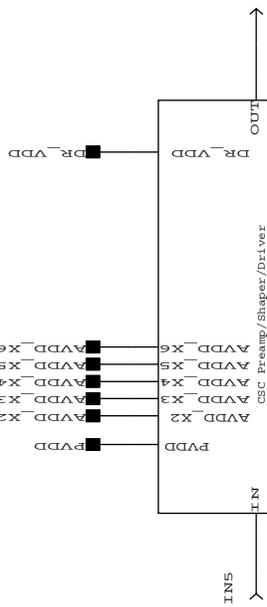
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ATLAS CSC / HP CMOS14TB 0.5U
CSC Preamp/Shaper 8 Channel bank

IC50

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Sheet: 1 of 3



Notes:

- P_VDD: 3.3V
- A_VDD: 3.3V
- DR_VDD: 3.3V
- A_GND: 0V
- DR_GND: 0V

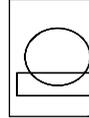
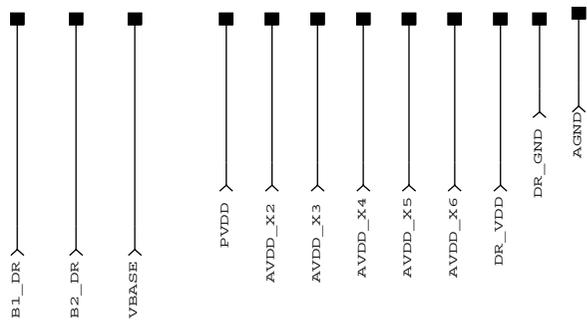
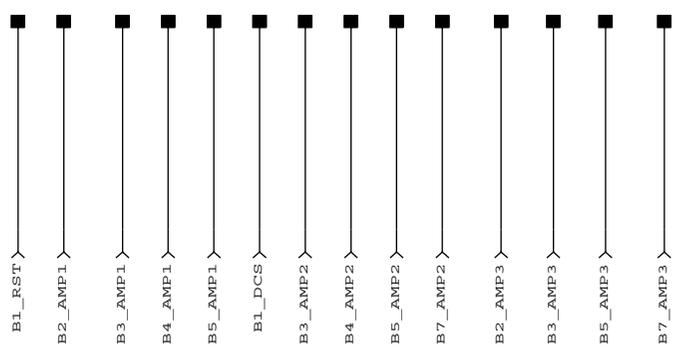
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ATLAS CSC / HP CMOS14TB 0.5U
CSC Preamp/Shaper 8 Channel bank

IC50

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Sheet: 2 of 3



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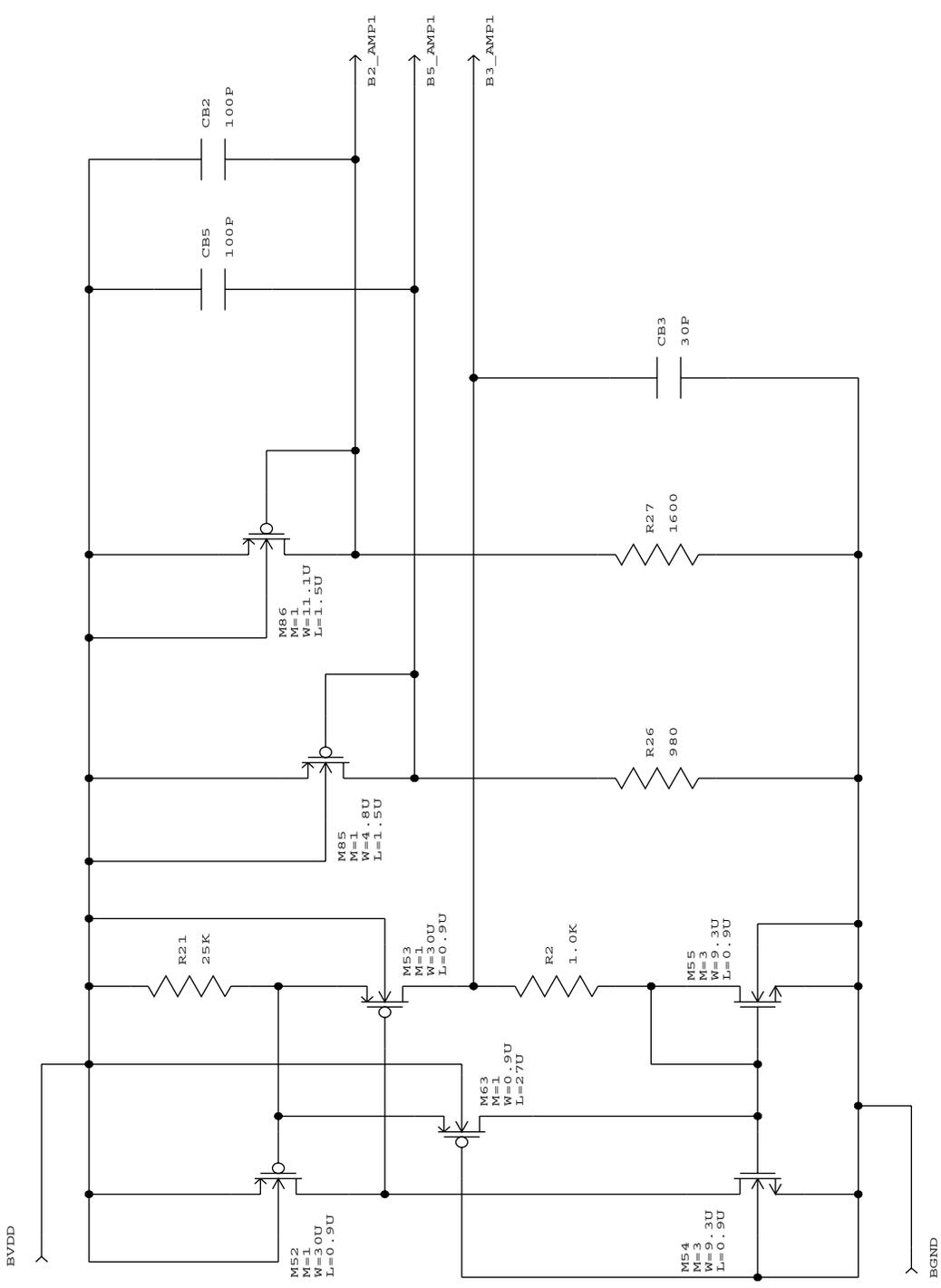
Drawn	
Checked	
Issued	
SIZE	B
DWG NO:	
REV NO:	1
SCALE	

Notes:

- FVDD: 3.3V
- AVDD: 3.3V
- DR_VDD: 3.3V
- AGND: 0V
- DR_GND: 0V

IC50

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Sheet: 3 of 3

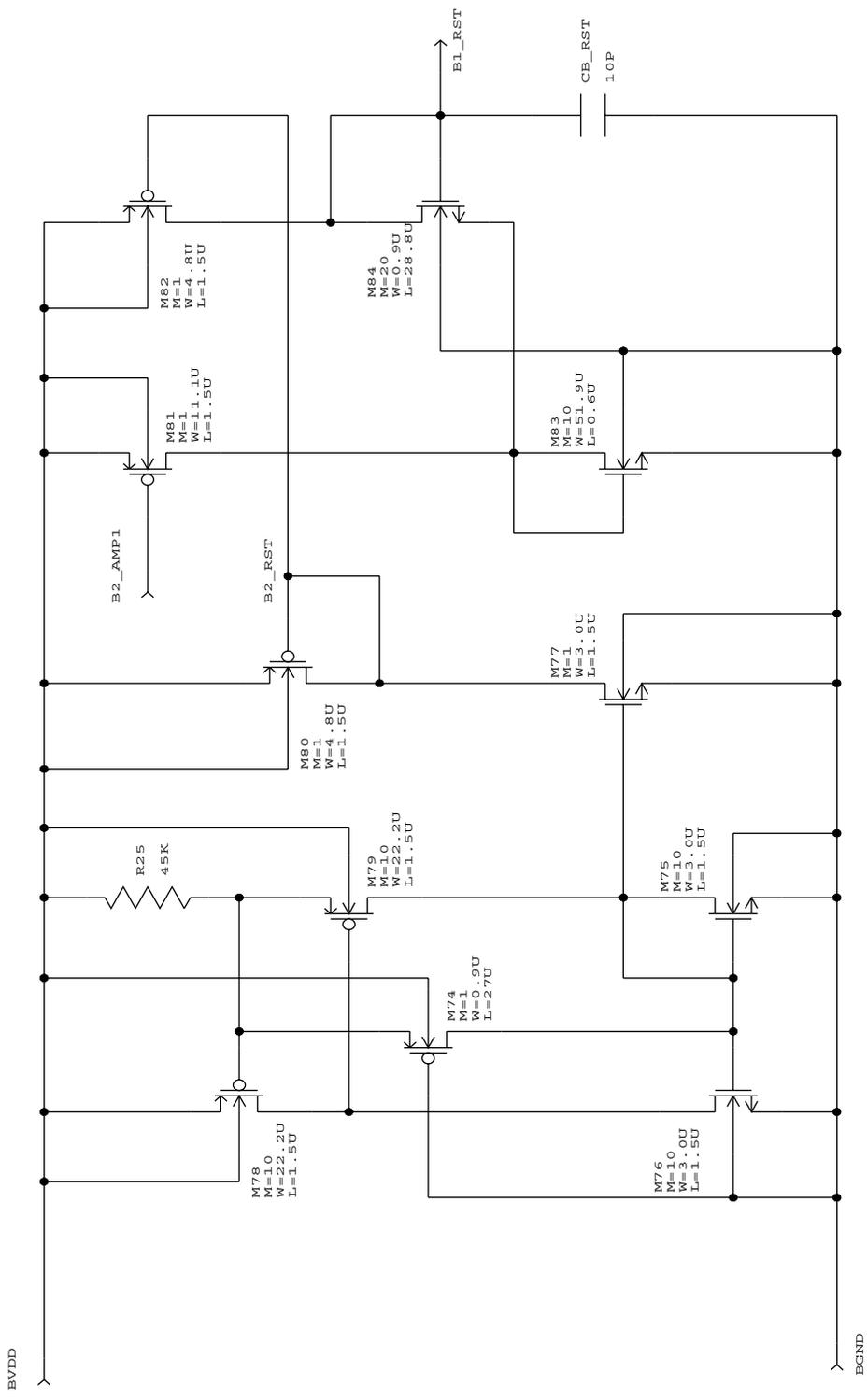


Notes:
 Changed the Following:
 M86 and M81 W=11.2U to 11.1U
 M83 and M55 W=52.01U to 51.9U
 B4_AMP1 NODE is GROUNDED at the AMP1 LEVEL

Bias lines:
 B1_RST
 B2_AMP1
 B3_AMP1
 B4_AMP1 ** is grounded at AMP1 level
 B5_AMP1

BVDD: 3.3V
 BGND: 0V

		Brookhaven National Laboratory Instrumentation Division Upton, NY 11973	
		ATLAS CSC / HP CMOS14TB 0.5U AMP1 and RESET BIAS	
Approvals	Date	Drawing:	
Drawn	Checked	Issued	
SIZE	B	Drawn By: Anand Kandasamy anandk@bnl.gov	
DWG NO:	1	Sheet: 1 of 2	
RET NO:	1	SCALE	



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		ATLAS CSC / HP CMOS14TB 0.5U AMP1 and RESET BIAS	
IC50		Drawn By: Anand Kandasamy Checked By: anandk@bnl.gov	
Drawn: _____ Checked: _____ Issued: _____		Drawings: _____	
APPROVALS	DATE	SCALE	
SIZE	B	DWG NO: 1	
RET NO:	1	SHEET: 2 of 2	

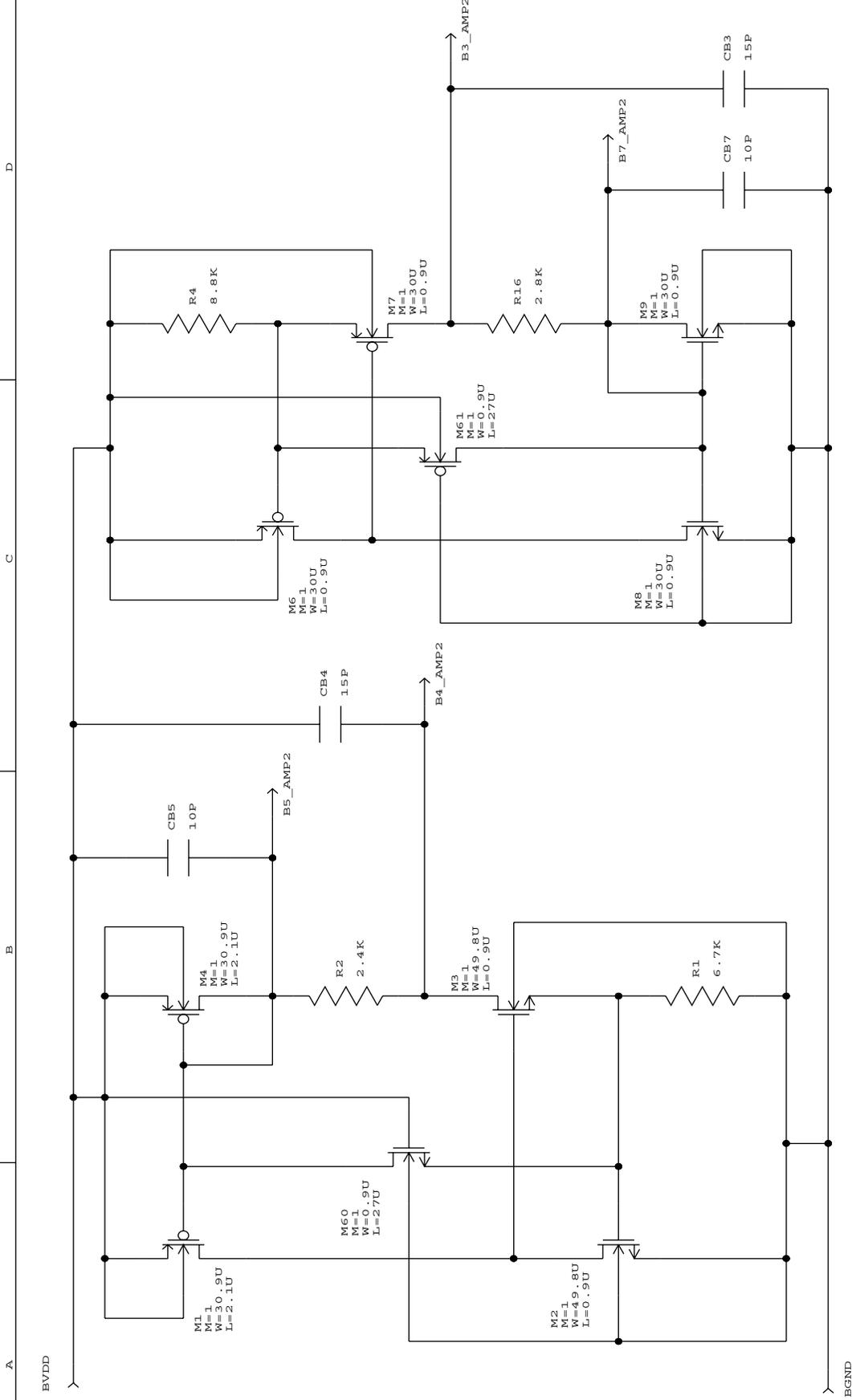
Notes:

Changed the Following:

M85 and M81 W=11.2U to 11.1U
 M83 and M55 W=52.01U to 51.9U
 B4_AMP1 NODE is GROUNDED at the AMP1 LEVEL

Bias lines:
 B1_RST
 B2_AMP1
 B3_AMP1
 B4_AMP1 ** is grounded at AMP1 level
 B5_AMP1

BVDD: 3.3V
 BGNDD: 0V



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		ATLAS CSC / HP CMOS14TB 0.5U AMP2-BIAS	
Approvals Date Drawing:		Drawn By: Anand Kandasamy anandk@bnl.gov	
Drawn		Scale: 1 of 1	
Checked		DWG NO: 1	
Issued		REV NO: 1	
SIZE: B		SCALE	

Notes:

Changed the Following:

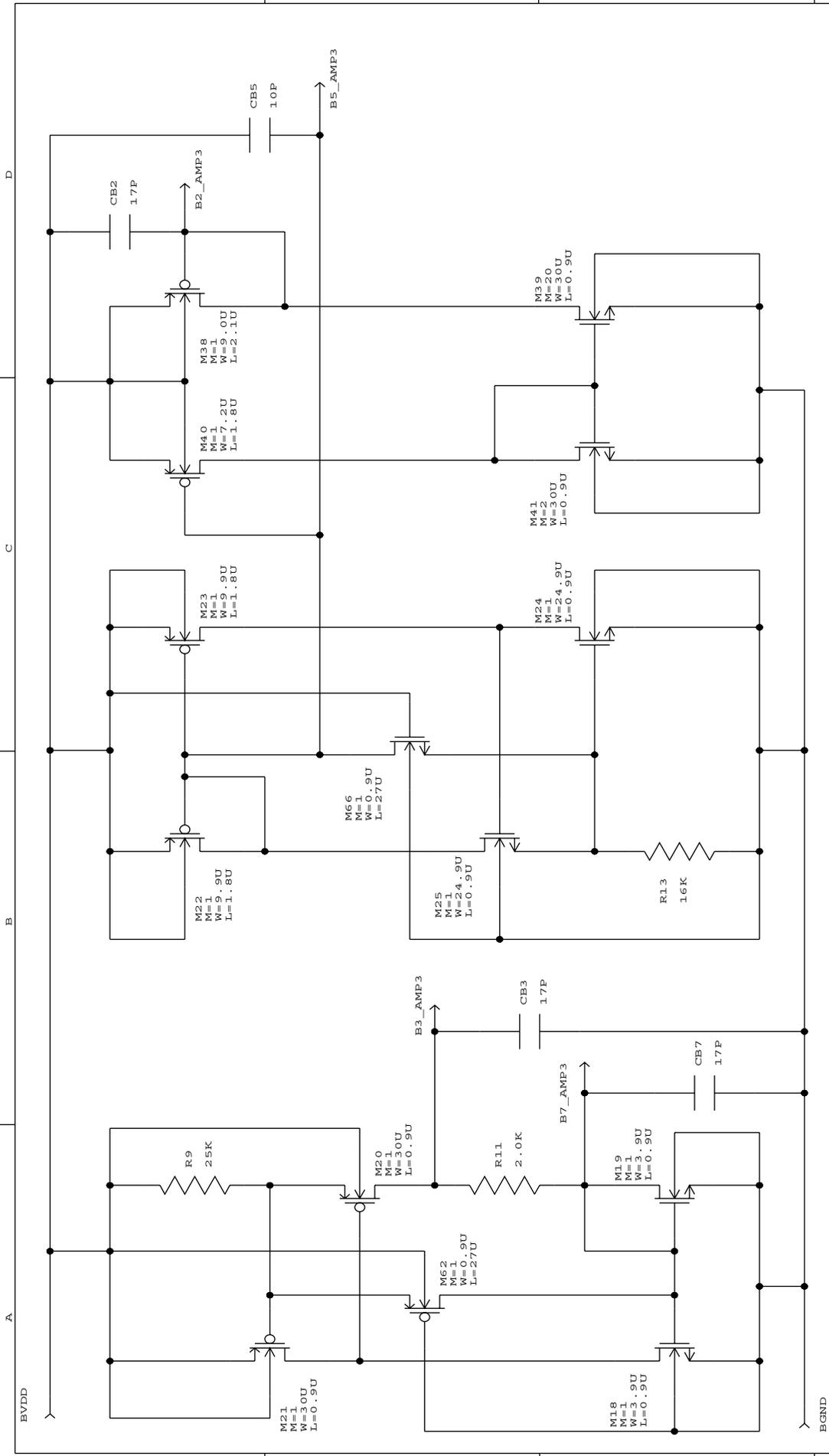
- M1 and M4 W=31U to 30.9U

Bias lines:

- B3_AMP2
- B4_AMP2
- B5_AMP2
- B7_AMP2

BVDD: 3.3V
 BGND: 0V

@DATEIME=5-26-1999_14:07
 @SHEET=1



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		Drawn By: Anand Kandasamy anandk@bnl.gov	
Approvals Date Drawings:		ATLAS CSC / HP CMOS14TB 0.5U AMP3-BIAS	
Drawn Checked Issued		SCALE: 1 of 1	
SIZE: B DWG NO: 1 REV NO: 1		<h1 style="text-align: center;">IC50</h1>	
SCALE			

Notes:
 Changed the Following:

Bias lines:
 B2_AMP3
 B3_AMP3
 B5_AMP3
 B7_AMP3

M22 and M23 W=9.8U to 9.9U
 M24 and M25 W=25U to 24.9U
 M38 W=9.1U to 9.0U

BVDD: 3.3V
 B5_AMP3: 0V

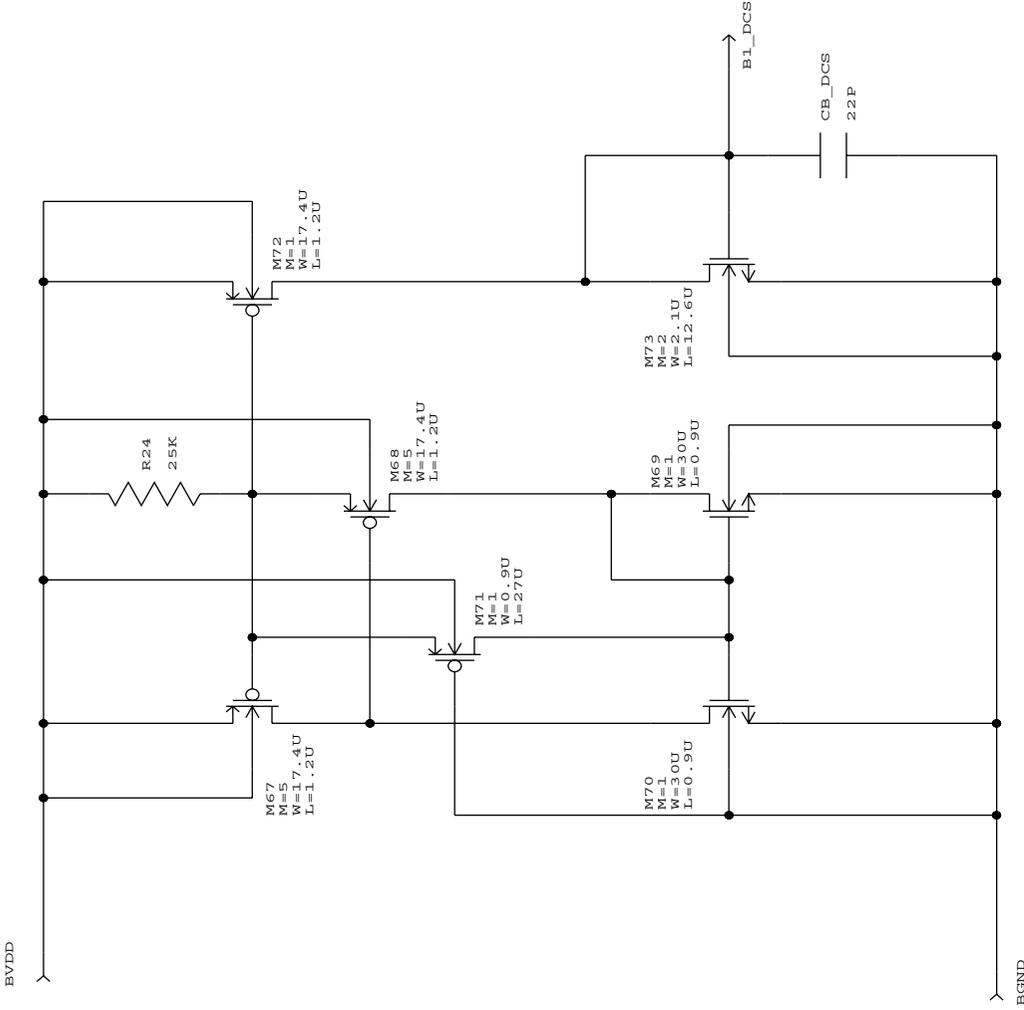
A

B

C

D

Bias lines:
BI_DCS
BYDD: 3.3V
BGND: 0V



Notes:

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Drawn		
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ATLAS CSC / HP CMOS14TB 0.5U
DC Control Bias

IC50

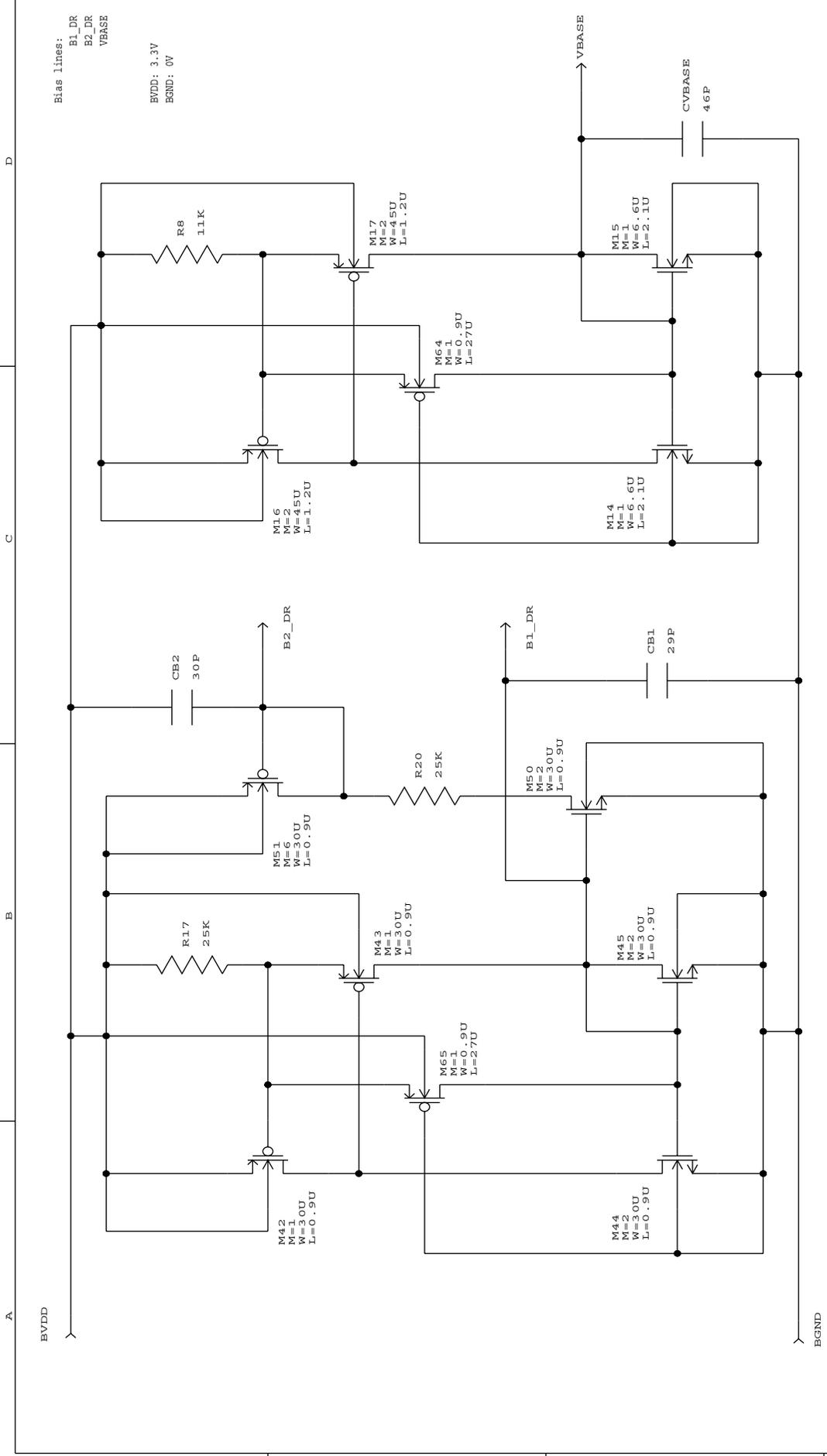
Drawn By: Anand Kandasamy
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Sheet: 1 of 1

A

B

C

D



Bias lines:
 B1_DR
 B2_DR
 VBASE

BVDD: 3.3V
 BGND: 0V

Approvals	Date	Drawn by:
Drawn		
Checked		
Issued		

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ATLAS CSC / HP CMOS14TB 0.5U
 CLASS AB DRIVER-BIAS

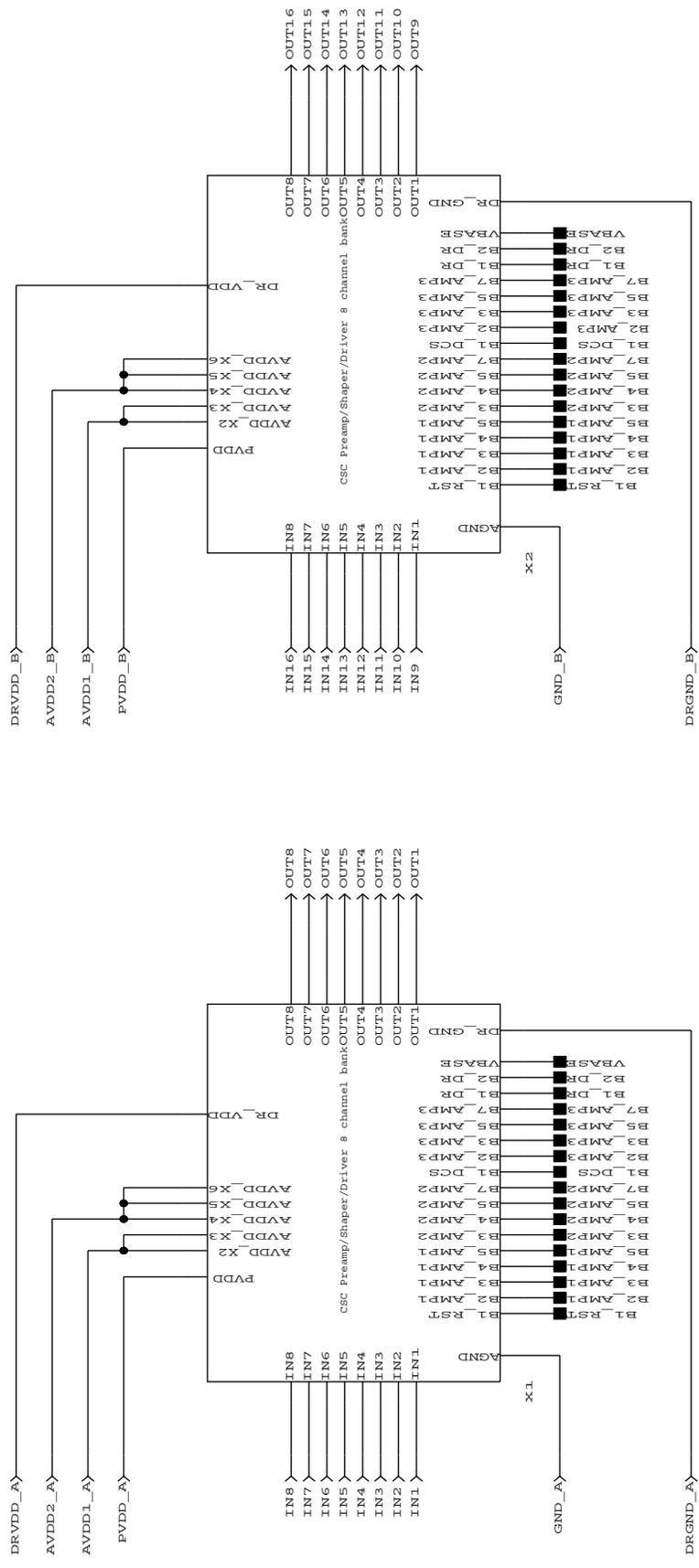
IC50

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Sheet: 1 of 1

Notes:

Changed the following:
 M67 and M17 : M=1, W=90U to M=2, W=45U





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Approvals		Drawings	
Drawn	Date	Checked	Date

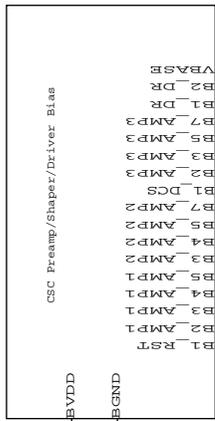
ATLAS CSC / HP CMOS14TB 0.5U
CSC - IC50 Die Structure

IC50

SIZE	B	Drawn By:	Anand Kandasamy
DWG NO:	1	Checked By:	anandk@bnl.gov
REV NO:	1	Issued By:	anandk@bnl.gov
SCALE		Sheet:	1 of 2

Notes:

PVPD_A, AVDD1_A, AVDD2_A, DRVDD_A : 3.3V
 PVPD_B, AVDD1_B, AVDD2_B, DRVDD_B : 3.3V
 GND_A, GND_B, EGNND, DRGND_A, DRGND_B : 0V



BVDD

BGND

X3

B1 RST
 B2 AMP1
 B3 AMP1
 B4 AMP1
 B5 AMP1
 B3 AMP2
 B4 AMP2
 B5 AMP2
 B7 AMP2
 B1 DCS
 B2 AMP3
 B3 AMP3
 B5 AMP3
 B7 AMP3
 B1 DR
 B2 DR
 VBASE

VBASE
 B2_DR
 B1_DR
 B7_AMP3
 B5_AMP3
 B3_AMP3
 B2_AMP3
 B1_DCS
 B7_AMP2
 B5_AMP2
 B4_AMP2
 B3_AMP2
 B5_AMP1
 B4_AMP1
 B3_AMP1
 B2_AMP1
 B1_RST

Notes:

- PVDD_A, AVDD1_A, AVDD2_A, DRVDD_A : 3.3V
- PVDD_B, AVDD1_B, AVDD2_B, DRVDD_B : 3.3V
- GND_A, GND_B, BGND, DRGND_A, DRGND_B : 0V



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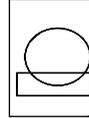
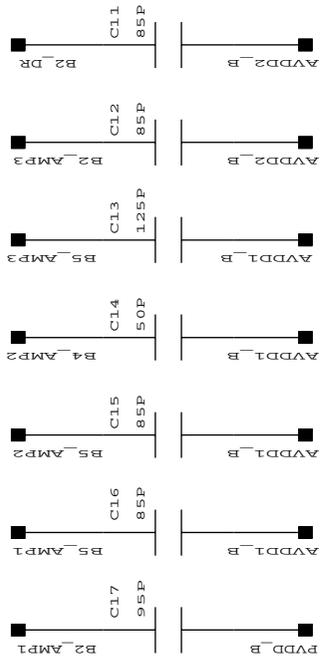
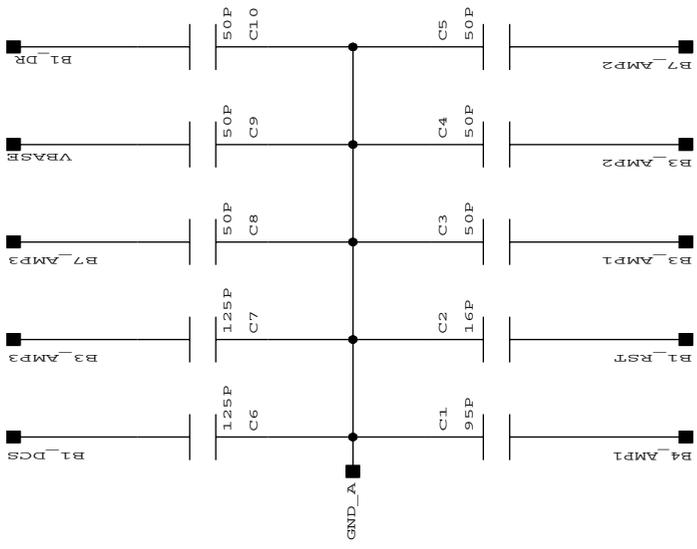
Approvals Date Drawings:

Approvals	Date	Drawings
Drawn		
Checked		
Issued		

ATLAS CSC / HP CMOS14TB 0.5U
 CSC - IC50 Die Structure

IC50

Drawn By: Anand Kandasamy
 anandk@bnl.gov
 Sheet: 2 of 2



Brookhaven National Laboratory
Instrumentation Division
Upton, NY 11973

Approvals	Date	Drawn by:
Drawn		
Checked		
Issued		

ATLAS CSC / HP CMOS14TB 0.5U
CSC - IC50

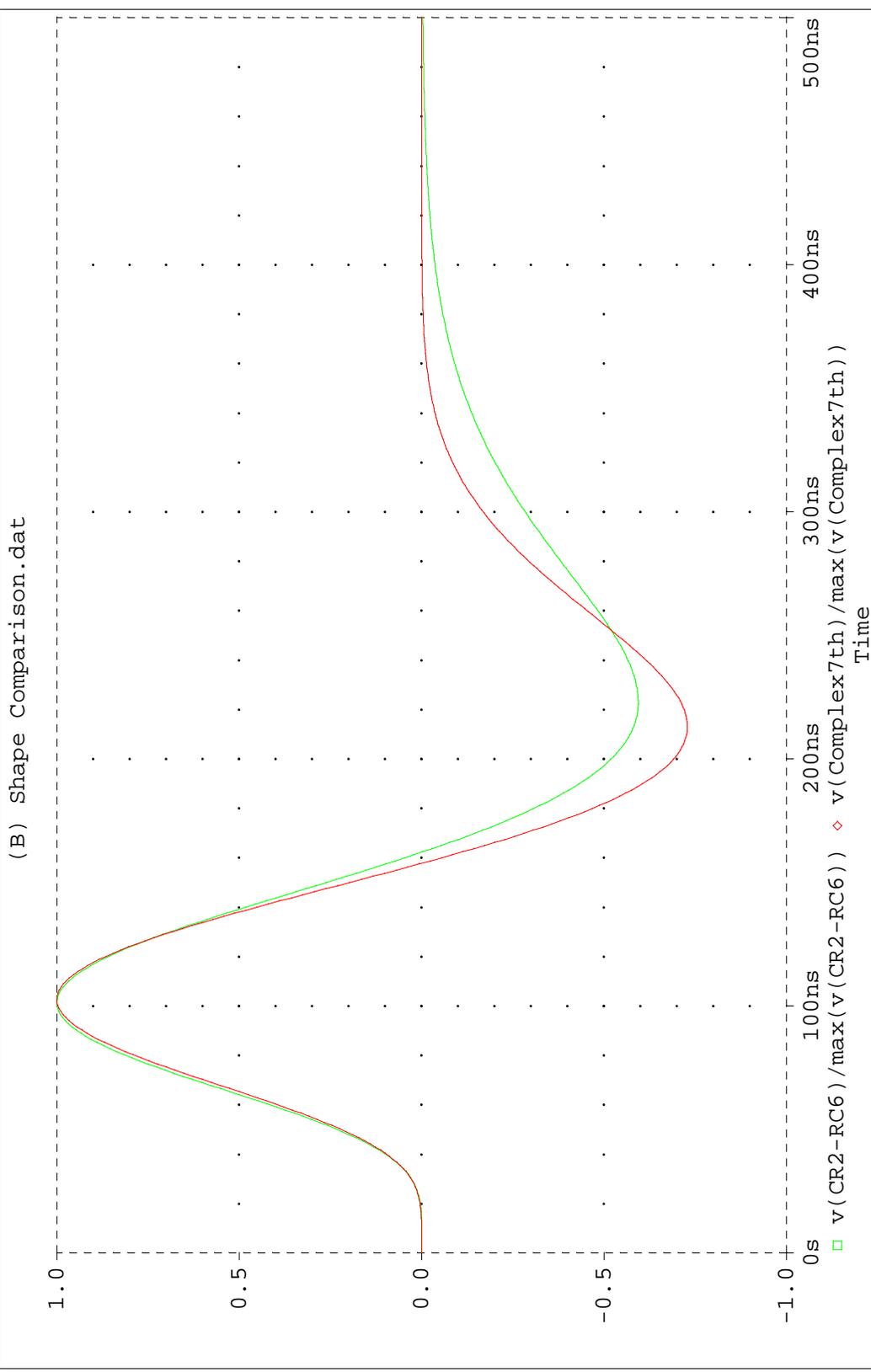
IC50

Drawn By: Anand Kandasamy
anandk@bnl.gov
Sheet: 2 of 2

Comparison of CR2-RC6 and complex 7th order shapers

Date/Time run: 05/12/99 15:57:15

Temperature: 27.0



Date: May 12, 1999

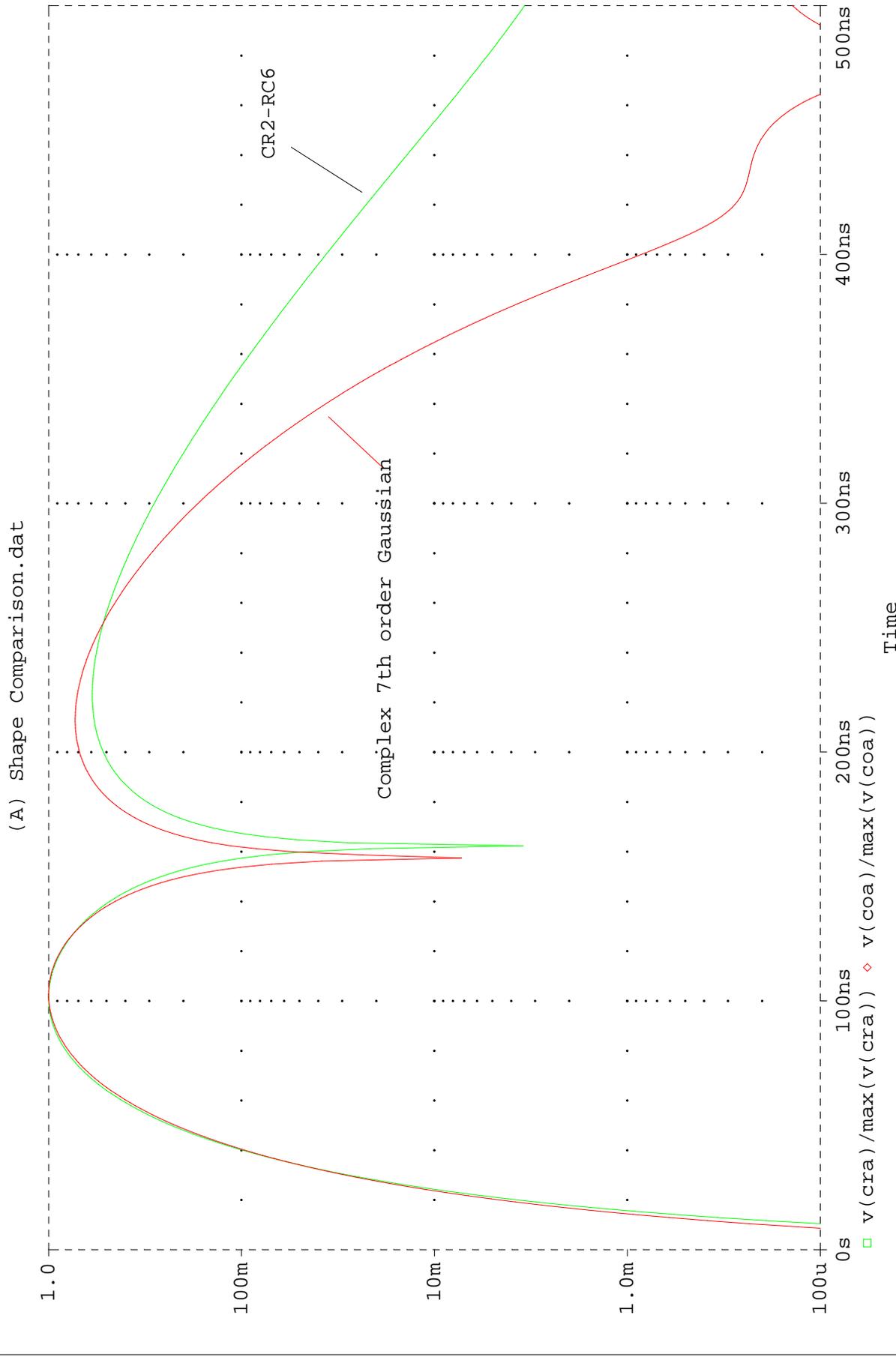
Page 1

Time: 15:59:17

Shape Comparison - Log Scale

Date/Time run: 05/12/99 15:57:15

Temperature: 27.0



A1:(448.148n,11.364m) A2:(362.963n,11.198m) DIFF(A):(85.185n,166.378u)

Date: May 12, 1999

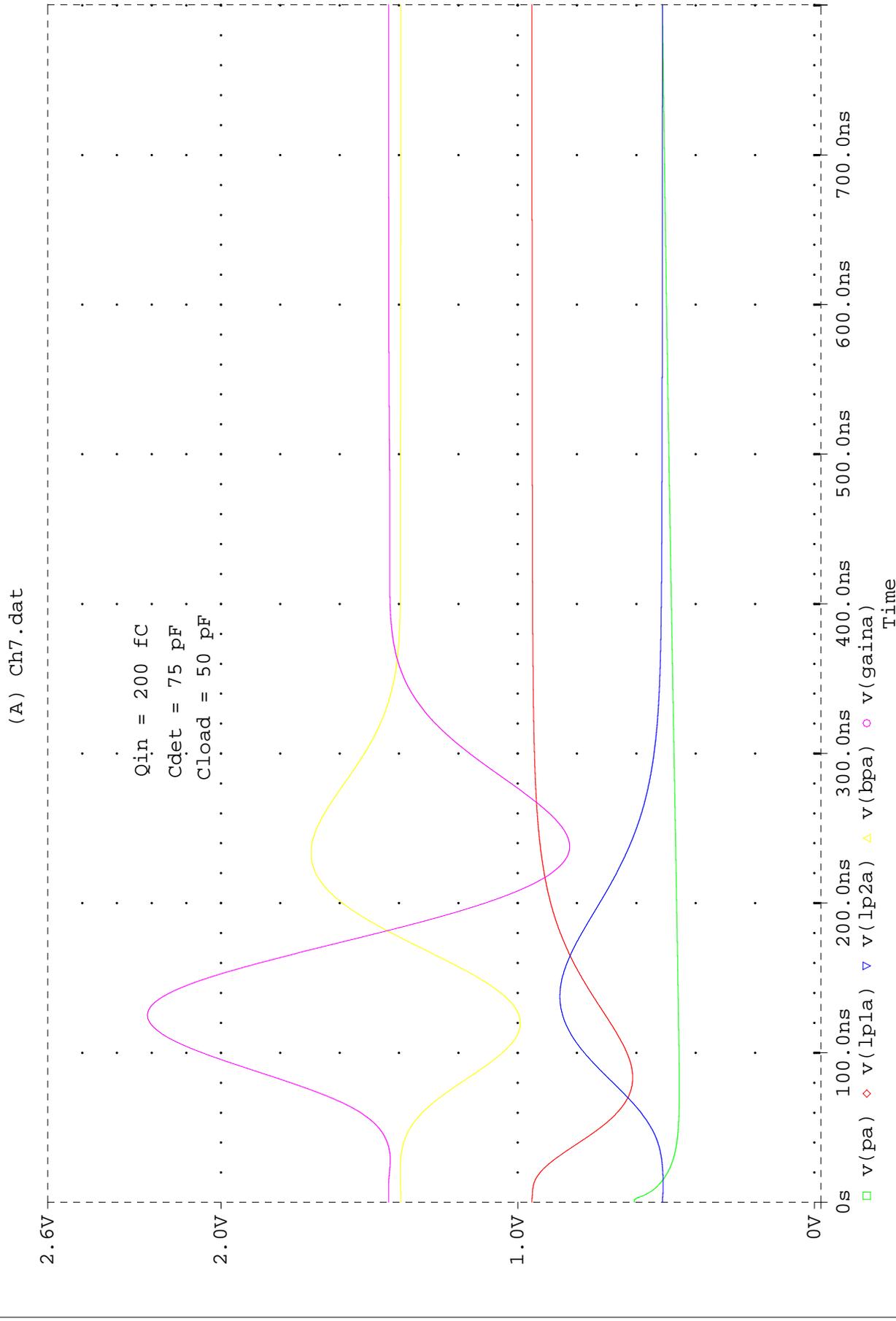
Page 1

Time: 16:15:44

Preamp, intermediate nodes, and output signals

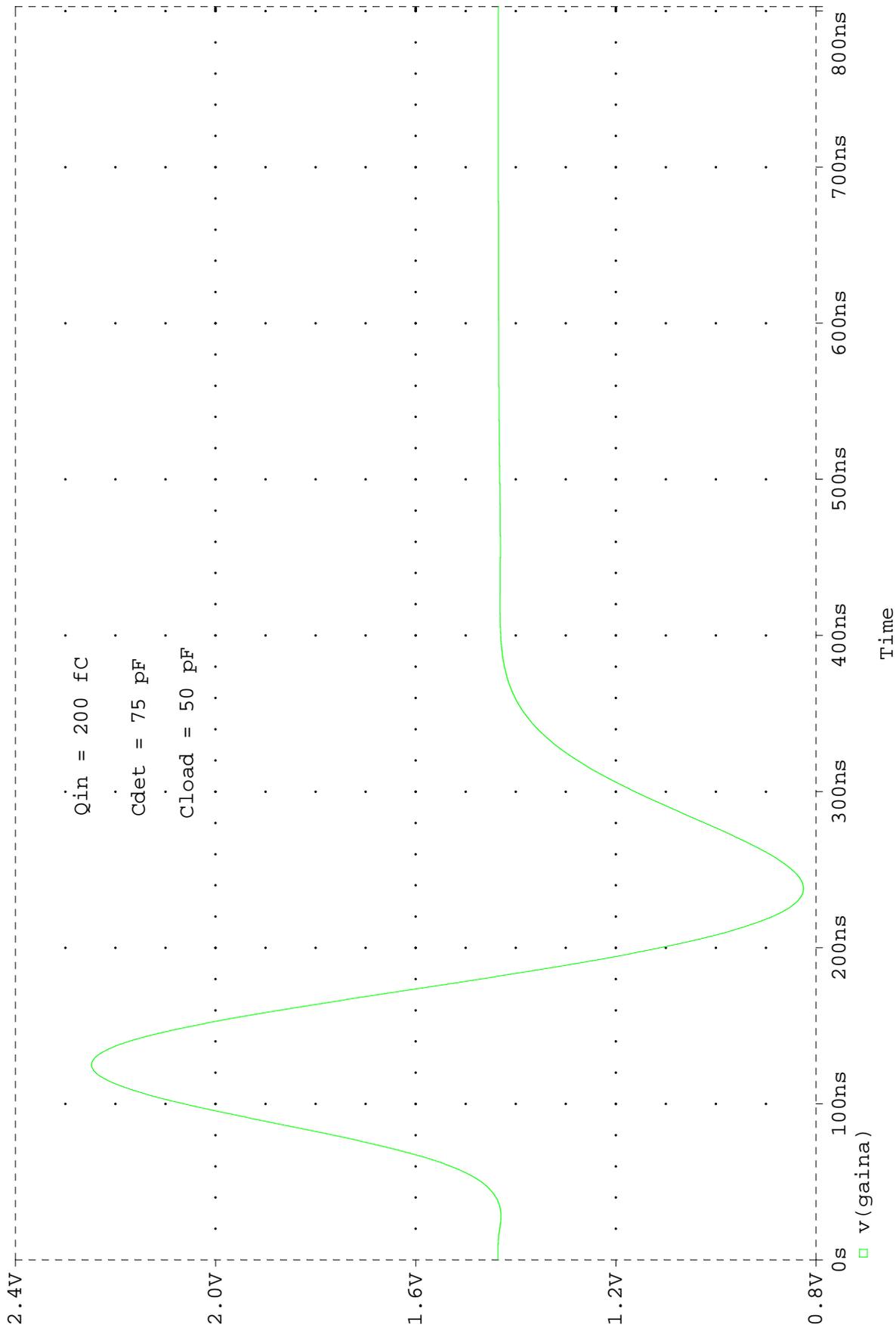
Date/Time run: 05/12/99 09:44:10

Temperature: 27.0



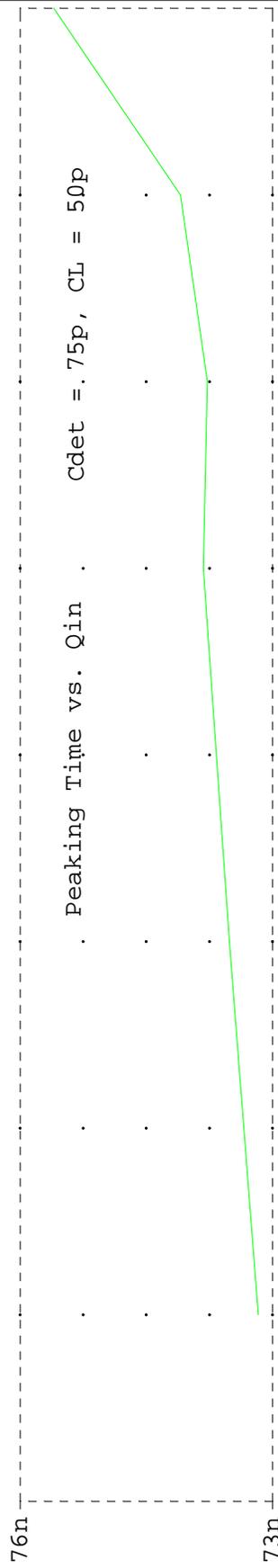
Output

(A) Ch7.dat

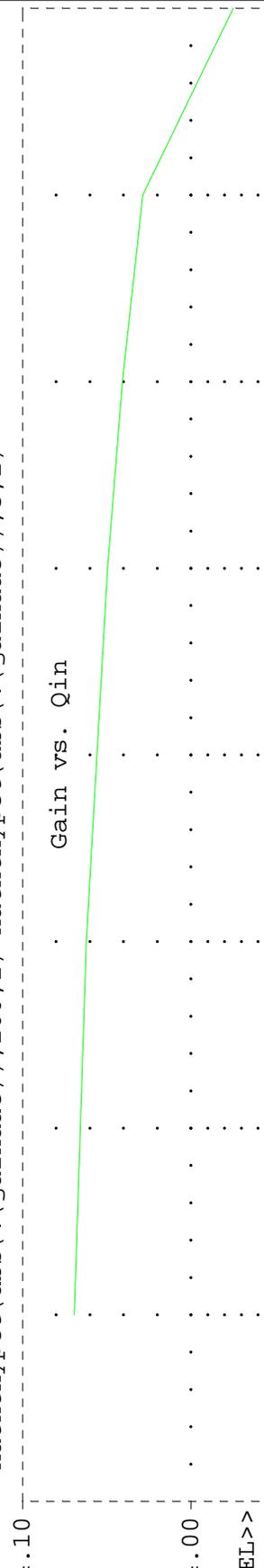


Linearity: Input charge 100 - 450 fC

(A) Ch7.dat

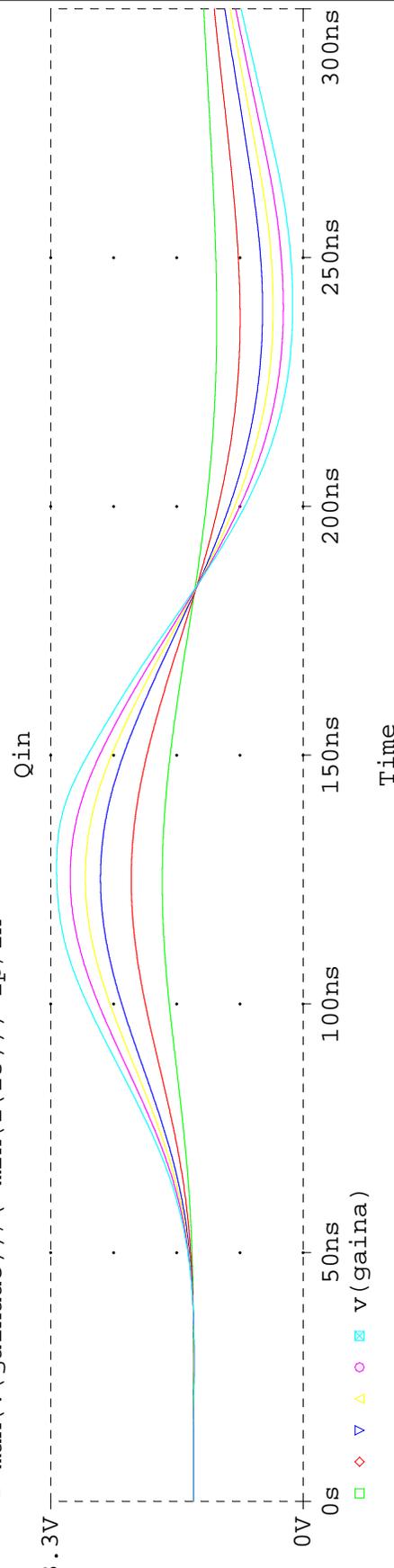


□ xatnthypct(abs(v(gainaac)),100,1)-xatnthypct(abs(v(gainaac)),5,1)



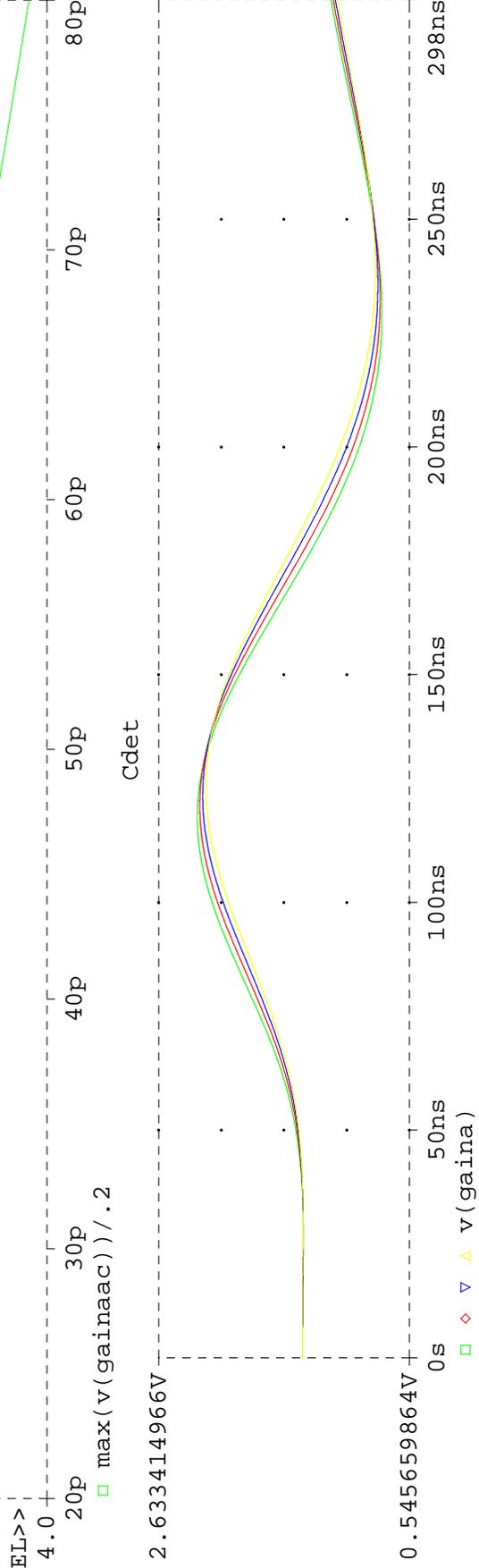
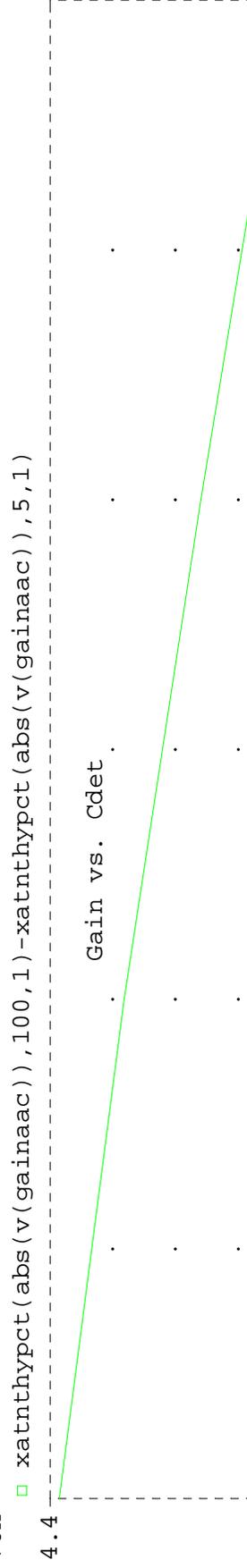
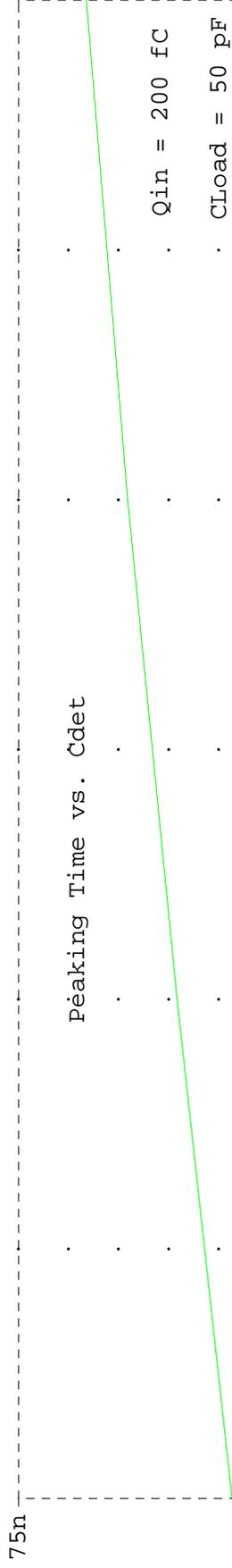
SEL>

□ max(v(gainaac))/(-min(i(i3)))*1p/2n



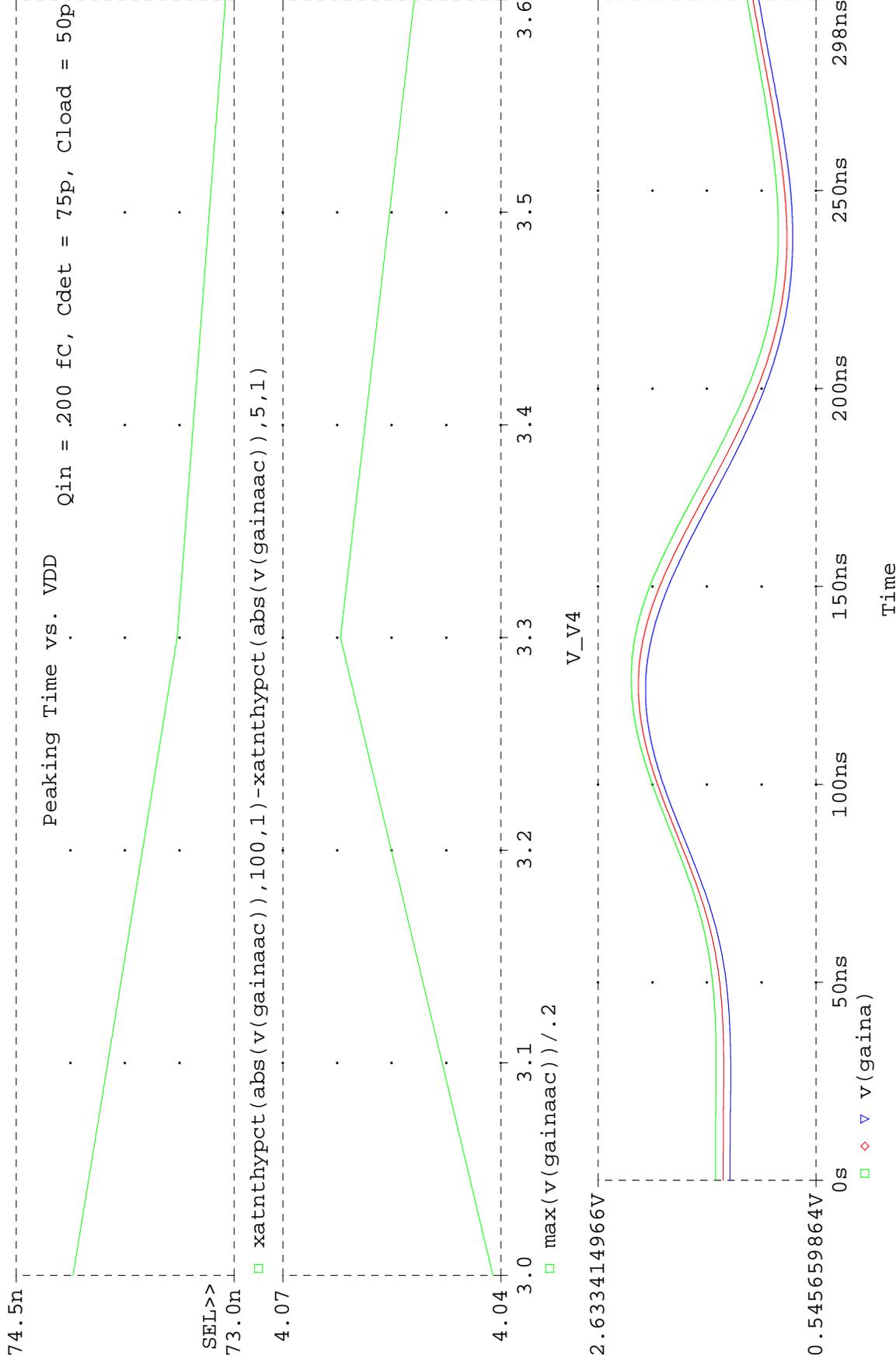
Variation of Cdet: 20 - 80 pF

(A) Ch7.dat



Variation of VDD: 3.0 - 3.6 V

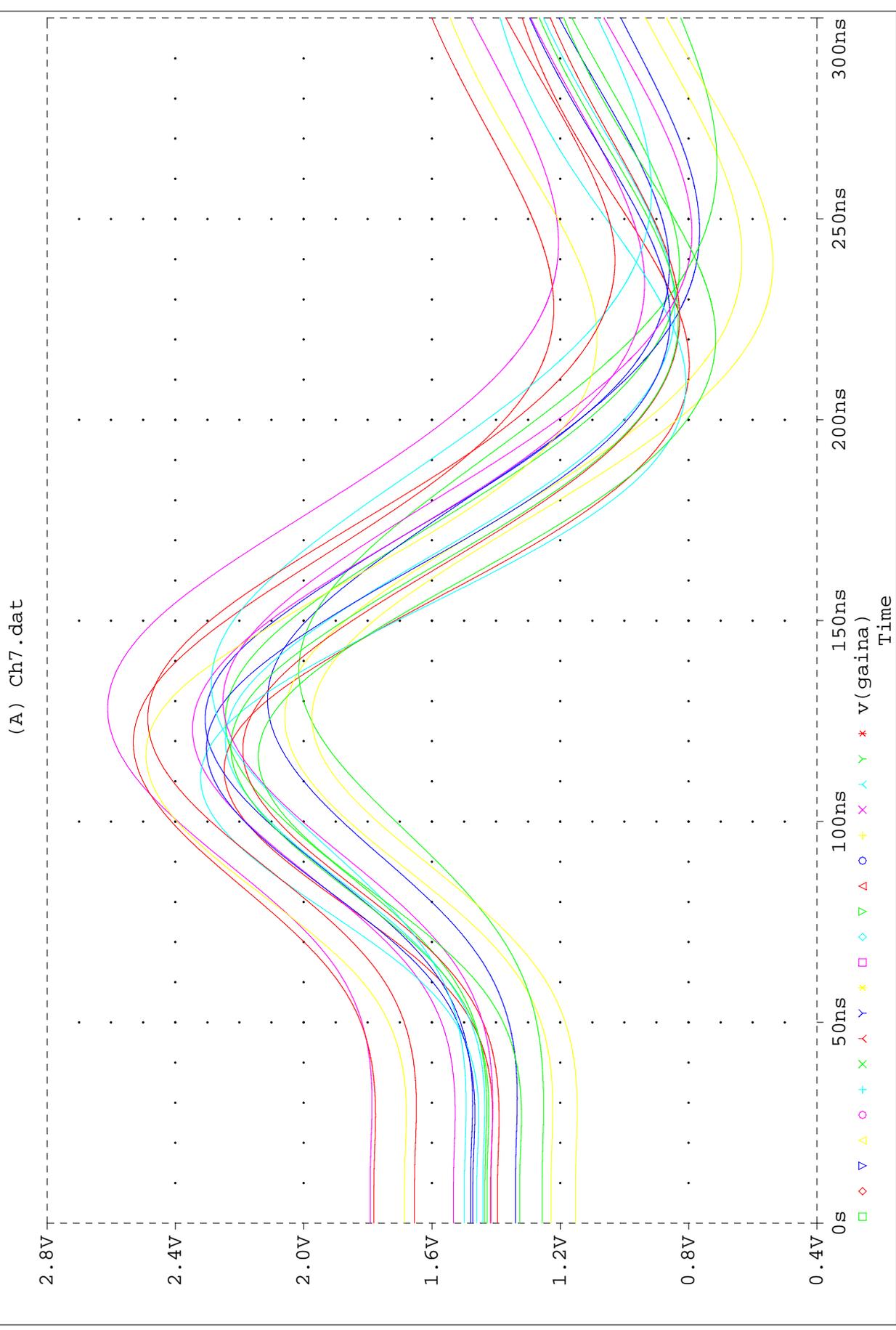
(A) Ch7.dat



Output Node

Date/Time run: 05/11/99 17:50:54

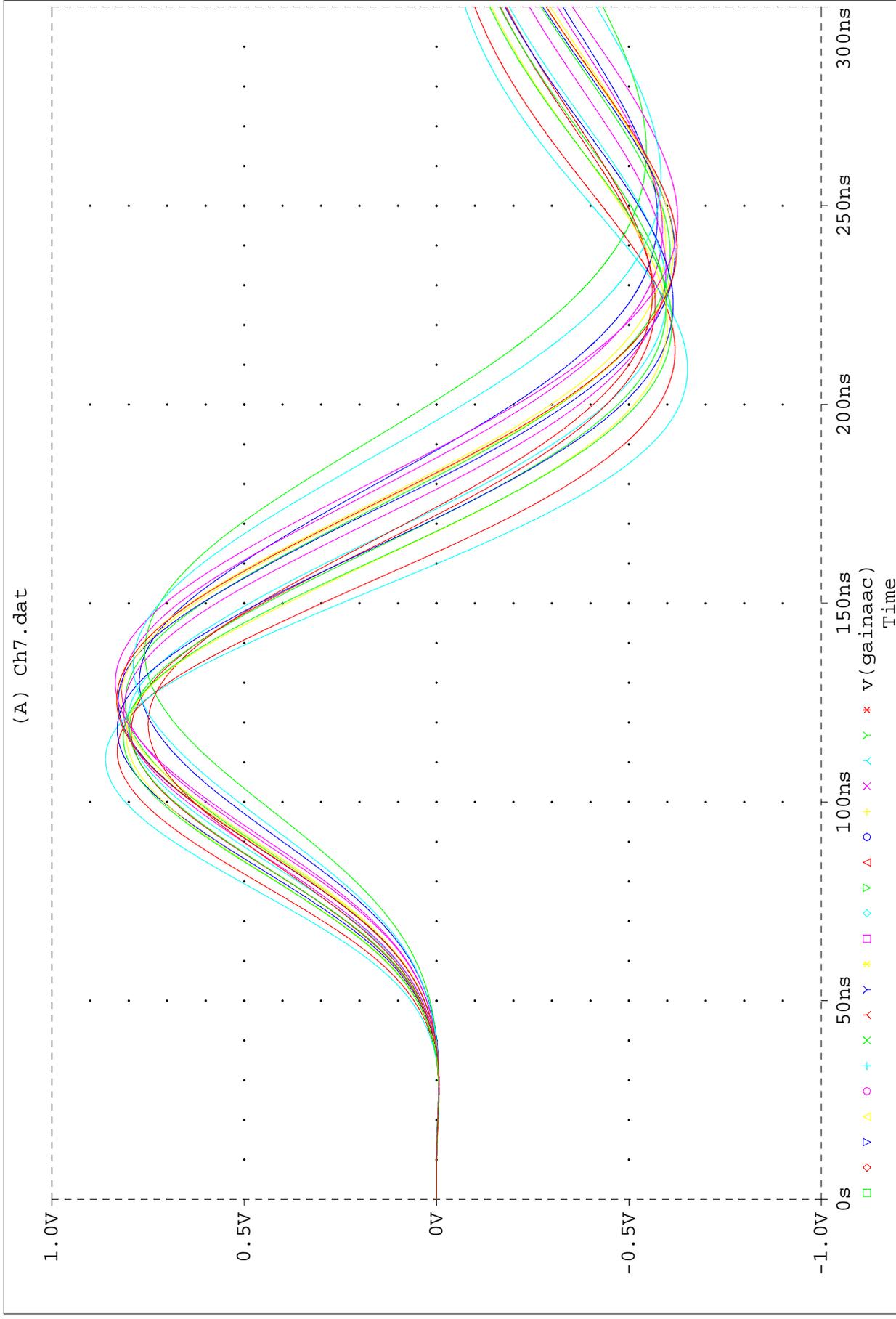
Temperature: 27.0

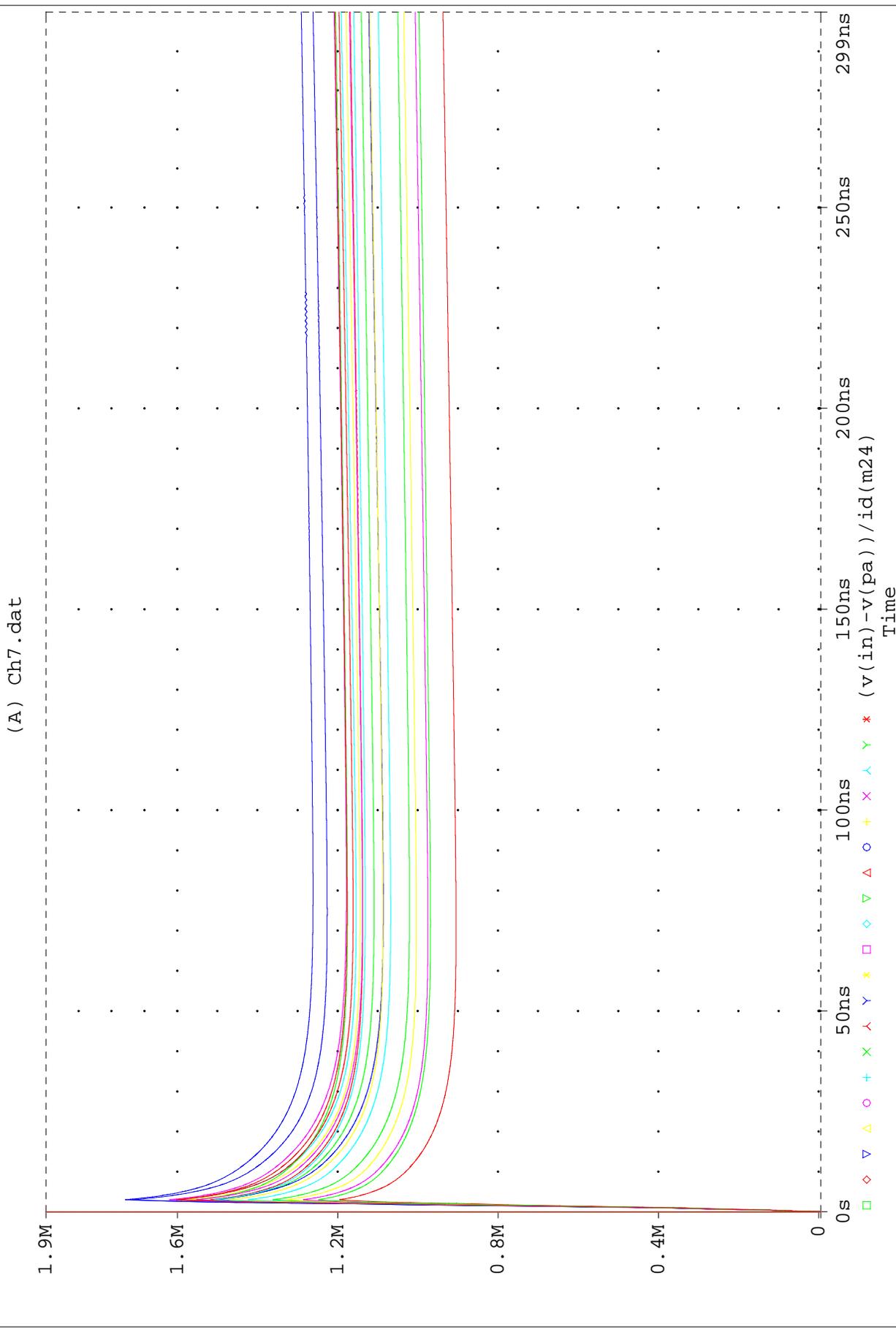


Output -- baseline subtracted

Date/Time run: 05/11/99 17:50:54

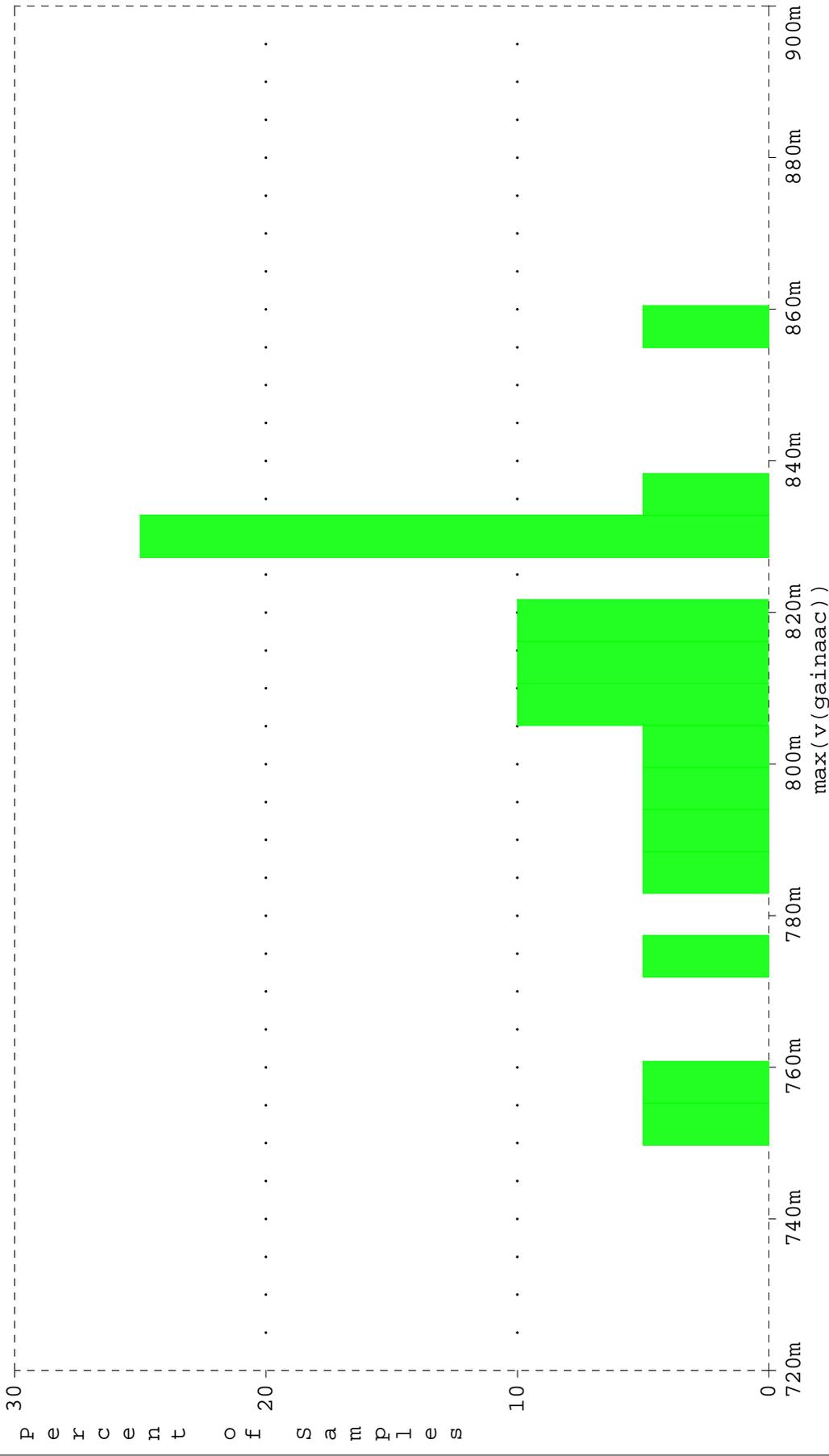
Temperature: 27.0



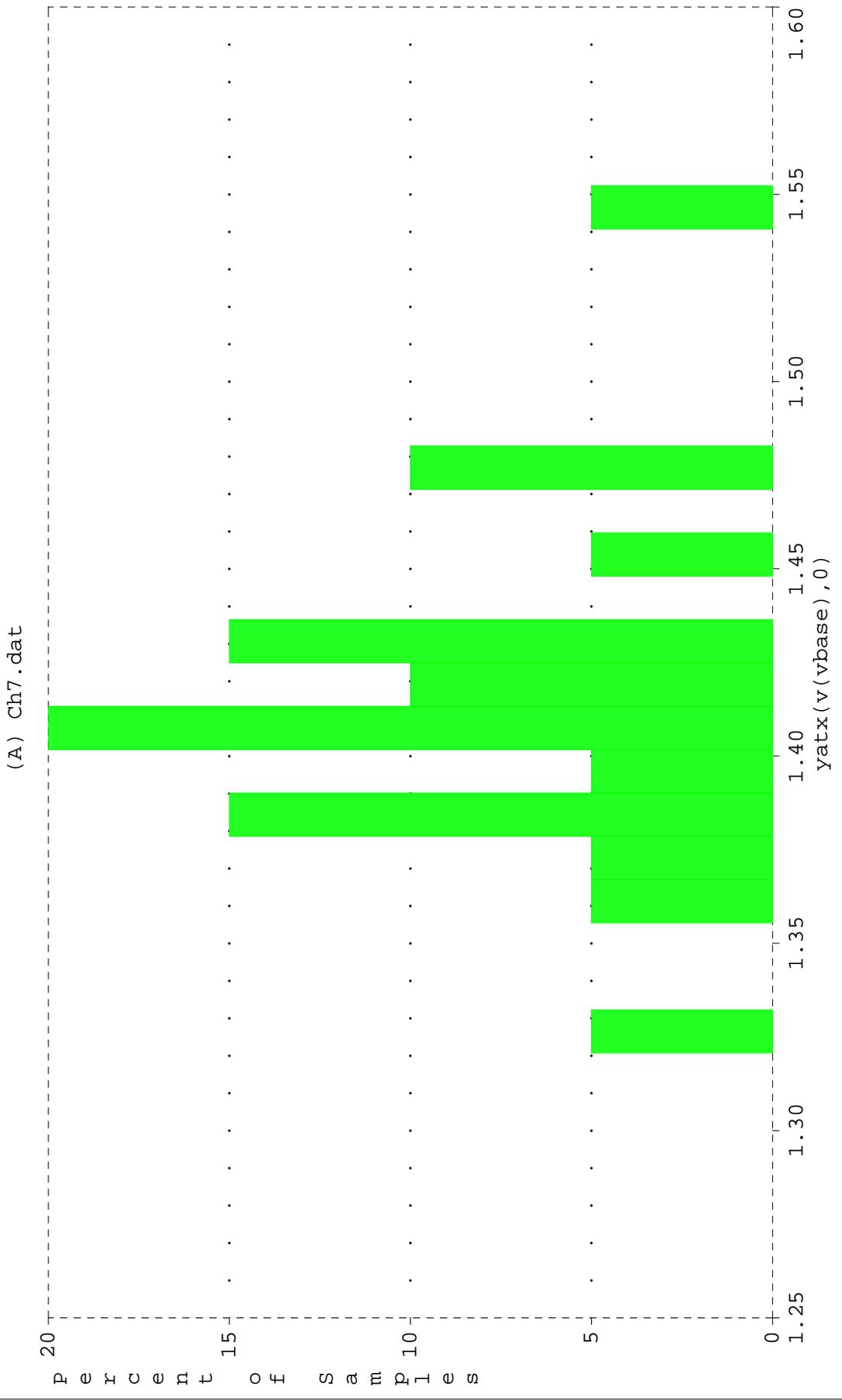


Gain Histogram

(A) Ch7.dat

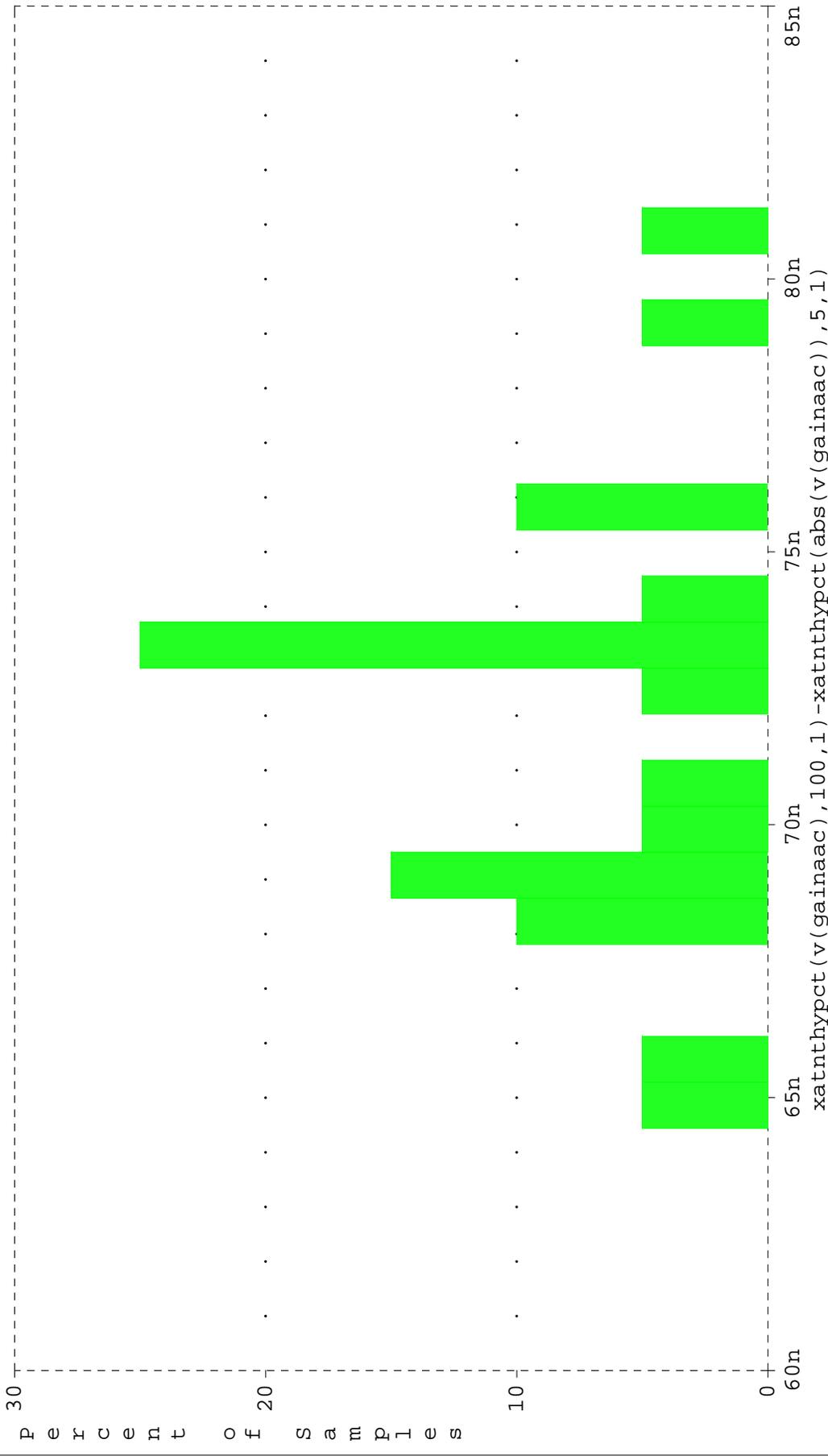


n samples	= 20	sigma	= 0.0271386	median	= 0.813749
n divisions	= 20	minimum	= 0.74971	90th %ile	= 0.833178
mean	= 0.809518	10th %ile	= 0.765622	maximum	= 0.860467



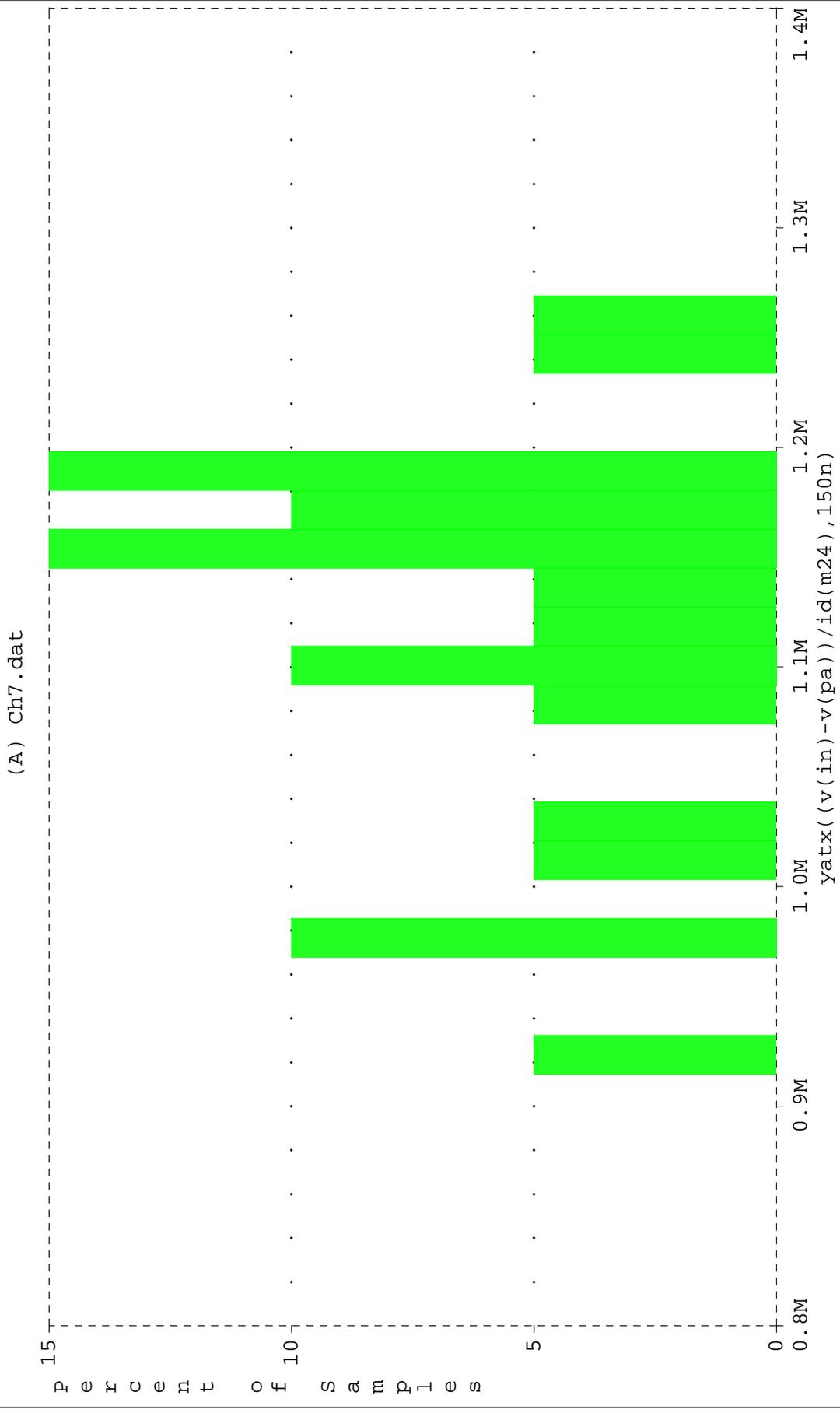
n samples	= 20	sigma	= 0.048995	median	= 1.41129
n divisions	= 20	minimum	= 1.32064	90th %ile	= 1.4723
mean	= 1.41517	10th %ile	= 1.36602	maximum	= 1.55229

(A) Ch7.dat



n samples	= 20	sigma	= 4.29903e-009	median	= 7.26138e-008
n divisions	= 20	minimum	= 6.44359e-008	90th %ile	= 7.77753e-008
mean	= 7.2022e-008	10th %ile	= 6.67434e-008	maximum	= 8.13059e-008

Feedback resistance histogram



n samples	= 20	sigma	= 91520.7	median	= 1.14273e+006
n divisions	= 20	minimum	= 914525	90th %ile	= 1.23595e+006
mean	= 1.11439e+006	10th %ile	= 914525	maximum	= 1.26903e+006